

## 1.2A 1.5MHz High Efficiency Synchronous-Rectified Step-Down Converter

### General Information

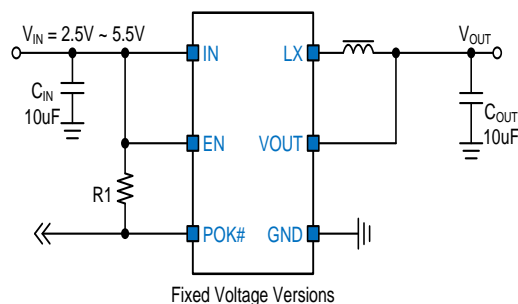
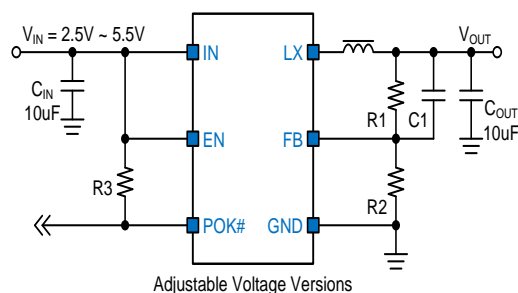
The LTS8002 is a synchronous step-down converter with an input voltage range of 2.5V to 5.5V. It delivers up to 1A continuous output current with high efficiency over a wide output current range. At medium to heavy load, the converter operates in PWM mode and automatically enters power save mode operation at light load currents to maintain high efficiency over the entire load current range.

The output voltage can be output voltage can be regulated as low as 0.6V. The LTS8002 can also run at 100% duty cycle for low dropout applications. The device enters shutdown mode and consumes less than 0.1uA when the EN pin is pulled low.

To address the requirements of system power rail, the internal compensation circuit allows a large selection of external capacitor values ranging from 10uF up to 100uF effective capacitance.

Other features include soft-start, 0.6V internal reference voltage with 2% accuracy, over temperature protection, and over current protection. The LTS8002 is available in TSOT23-5, TSOT23-6, or WDFN2x2-6L package.

### Typical Application Circuit



### Features

- Wide Input Voltage from 2.5V to 5.5V
- Adjustable Output Voltage form 0.6V to  $V_{IN}$
- 100% Duty Cycle for Lowest Dropout
- 1.2A Output Current
- Up to 95% High Efficiency
- No Schottky Diode Required
- 1.5MHz Fixed Frequency PWM Operation
- Power Save Mode for Light Load Efficiency
- Output Discharge Function
- Power Good Output
- TSOT23-5, TSOT23-6 or WDFN2x2-6L Package
- RoHS Compliant and Halogen Free

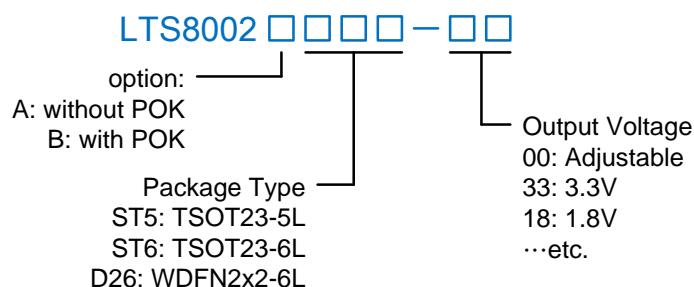
### Applications

- Battery Powered Portable Devices
- Point of Load Regulators
- System Power Rail Voltage Conversion
- Cellular Phones
- Personal Information Appliances

### Pin Configuration & Top Marking

Pin Configuration	Top Marking
<p>TSOT23-5 (AST5)</p>	<p>PPPP: Product Code YMDS: Date Code</p>
<p>TSOT23-6 (BST6)</p>	<p>PPPP: Product Code YMDS: Date Code</p>
<p>WDFN2x2-6L (BD26)</p>	<p>PPPP: Product Code YMDS: Date Code</p>

## Ordering Information



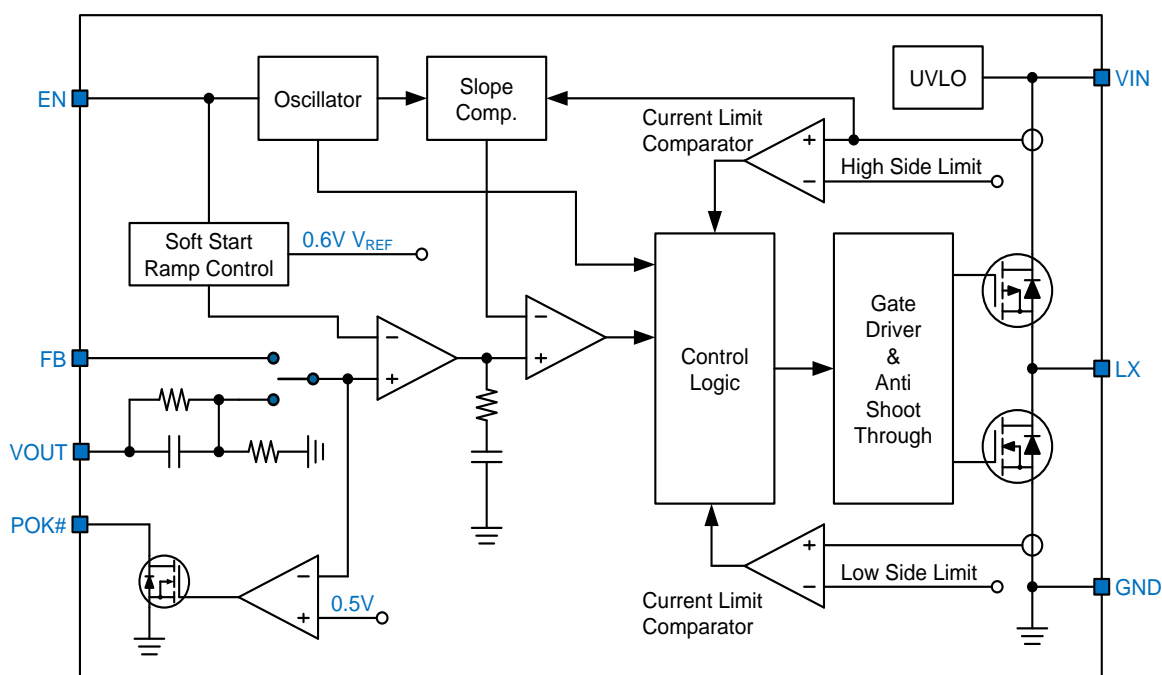
Ordering Number	Package	Top Marking	Note
LTS8002AST5-00	TSOT23-5	SK	Adjustable Output Voltage
LTS8002AST5-33	TSOT23-5	SL	3.3V Output Voltage
LTS8002AST5-25	TSOT23-5	SM	2.5V Output Voltage
LTS8002AST5-18	TSOT23-5	SN	1.8V Output Voltage
LTS8002AST5-15	TSOT23-5	SO	1.5V Output Voltage
LTS8002AST5-12	TSOT23-5	SP	1.2V Output Voltage
LTS8002BST6-00	TSOT23-6	SR	Adjustable Output Voltage, with POK
LTS8002BST6-33	TSOT23-6	SS	3.3V Output Voltage, with POK
LTS8002BST6-25	TSOT23-6	ST	2.5V Output Voltage, with POK
LTS8002BST6-18	TSOT23-6	SV	1.8V Output Voltage, with POK
LTS8002BST6-15	TSOT23-6	SW	1.5V Output Voltage, with POK
LTS8002BST6-12	TSOT23-6	SX	1.2V Output Voltage, with POK
LTS8002BD26-00	WDFN2x2-6L	SY	Adjustable Output Voltage, with POK
LTS8002BD26-33	WDFN2x2-6L	T1	3.3V Output Voltage, with POK
LTS8002BD26-25	WDFN2x2-6L	T2	2.5V Output Voltage, with POK
LTS8002BD26-18	WDFN2x2-6L	T3	1.8V Output Voltage, with POK
LTS8002BD26-15	WDFN2x2-6L	T4	1.5V Output Voltage, with POK
LTS8002BD26-12	WDFN2x2-6L	T5	1.2V Output Voltage, with POK

Note 1. Leading TECH products are RoHs compliant and compatible with the current requirement of IPC/JDEC J-STD-020 and are suitable for use in SnPb or Pb-Free soldering processes.

## Functional Pin Descriptions

Pin Number			Pin Name	Description
AST5	BST6	BD26		
1	1	6	EN	<b>Enable Input.</b> Logic high turns on the converter. Do not let floating.
2	2	5	GND	<b>Ground.</b> Connect externally to thermal pad.
3	3	4	LX	<b>Switch Pin</b> connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter here.
4	4	3	VIN	<b>Power Supply Voltage Input.</b>
--	5	2	POK#	<b>Power OK Open Drain Output.</b> This pin is pulled to low if the FB voltage exceeds the rising threshold 89% of $V_{REF}$ . Let this pin floating if not used.
5	6	1	VOUT	<b>Output Voltage Sense Pin.</b> For fixed output versions only. Connect this pin the output voltage.
			FB	<b>Output Feedback Pin.</b> For adjustable output versions only. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT} = 0.6V \times (1 + R1/R2)$ . Add optional C1 (10pF ~ 47pF) to speed up transient response.
x	x	Thermal Pad	TP	<b>Ground.</b> Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect the thermal pad to ground plane or island with multiple through holes. For WDFN package only.

## Functional Block Diagram



## Operation Principles

The LTS8002 is a synchronous step-down converter with an input voltage range of 2.5V to 5.5V. It delivers up to 1A continuous output current with high efficiency over a wide output current range. At medium to heavy load, the converter operates in PWM mode and automatically enters power save mode operation at light load currents to maintain high efficiency over the entire load current range.

The output voltage can be output voltage can be regulated as low as 0.6V. The LTS8002 can also run at 100% duty cycle for low dropout applications. The device enters shutdown mode and consumes less than 0.1uA when the EN pin is pulled low.

To address the requirements of system power rail, the internal compensation circuit allows a large selection of external capacitor values ranging from 10uF up to 100uF effective capacitance.

Other features include soft-start, 0.6V internal reference voltage with 2% accuracy, over temperature protection, and over current protection. The LTS8002 is available in TSOT23-5, TSOT23-6, or WDFN2x2-6L package.

### Supply Input & Under Voltage Lockout (UVLO)

The LTS8002 operates with a wide input voltage range between 2.5V to 5.5V. The input voltage is continuously monitored for under voltage lockout (UVLO). UVLO shuts down the converter if the input voltage is lower than 2.4V threshold level.

The LTS8002 draws pulsed current with sharp edges each time the upper switch turns on, resulting in voltage ripples and spikes at supply input. A minimum 4.7uF ceramic capacitor with shortest PCB trace is highly recommended for bypassing the supply input.

### Supply Input & Under Voltage Lockout (UVLO)

Logic low at EN input shuts down the converter and reduces its quiescent to less than 1uA. In shutdown mode, both upper and lower switches are turned off.

Pulling the EN pin higher than 1.4V enables the converter and initiates the soft start cycle. The internal soft start circuitry controls output voltage ramping-up time (100us) to limits the inrush current at start-up. This prevents unwanted shutdown otherwise may be triggered by voltage drop due to large inrush current.

### PWM Operation

The LTS8002 adopts slope-compensated, current mode PWM control capable of achieving 100% duty cycle. During normal operation, the LTS8002 operates at PWM

mode to regulate output voltage by transferring the input power to the output voltage cycle by cycle at a constant 1.5MHz frequency.

The LTS8002 turns on the upper switch at each rising edge of the internal clock allowing the inductor current to ramp up linearly. The upper switch remains on until either the current-limit is tripped or the PWM comparator turns off the switch for regulating the output voltage. After the upper switch turns off, the lower switch turns on and free-wheels the inductor current until the rising edge of next clock. The inductor current ramps down linearly when upper switch turns off.

The LTS8002 regulates the output voltage by controlling the ramp up/down duty cycle of inductor current. The upper switch current is sensed, slope compensated and compared with the error amplifier output COMP to determine the adequate duty cycle. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.6V reference, which in turn, causes the COMP voltage to increase until the average inductor current matches the new load current.

### 100% Duty Cycle Low Dropout Mode

The LTS8002 increases duty cycle to maintain output voltage within regulation as the supply input drops gradually in battery-power application. The LTS8002 operates with 100% duty cycle and enters low dropout mode as the supply input approaches the output voltage. This maximizes the operation time by taking full advantage of the whole battery voltage range.

### Output Voltage Setting and Feedback Network

For the adjustable versions, the output voltage can be set from  $V_{REF}$  to  $V_{IN}$  by voltage dividers as:

$$V_{OUT} = V_{REF} \times \frac{R1 + R2}{R2}$$

The internal  $V_{REF}$  is 0.6V with 1.5% accuracy. For best accuracy,  $R2$  should be kept smaller than 40k $\Omega$  to ensure that the current flowing through  $R2$  is at least 100 times larger than  $I_{FB}$ . Changing the sum towards a lower value increases the robustness against noise injection. Changing the sum towards higher values reduces the quiescent current.

In real applications, a 22pF feed forward ceramic capacitor is recommended in parallel with  $R2$  for better transient response. The feed forward is internally implemented for the fixed voltage versions.

### ***POK# Output***

POK# is an open-drain output that indicates whether the output voltage is ready or not. POK# is typically pulled up to system I/O voltage level or tied with VIN directly. POK# is in low impedance when the voltage on FB pin exceeds the rising threshold 89% of V<sub>REF</sub>. POK# is in high impedance when the voltage on FB pin falls below the falling threshold 86% of V<sub>REF</sub>. If the voltage detector feature is not required, let this pin at floating state.

### ***Output Discharge***

The output gets discharged by the LX pin with a typical discharge resistor of R<sub>DIS</sub> whenever the device shuts down. This is the case when the device gets disabled by enable, thermal shutdown trigger, and under voltage lockout trigger.

### ***Current Limit***

Both upper and lower switches are short-circuit protected with maximum switch current = I<sub>LIM</sub>. The current in the switches is monitored by current limit comparators. Once the current in the upper switch exceeds the threshold of its current limit comparator, it turns off and the lower switch is activated to ramp down the current in the switch inductor and upper switch. The upper switch can only turn on again, once the current has decreased below the threshold of its current limit comparator.

If the load continuously demands more current than what LTS8002 could provide, it cannot regulate the output voltage. Eventually under voltage protection will be triggered and shuts down the LTS8002 if V<sub>OUT</sub> is too low.

### ***Under voltage Lockout (UVLO)***

Under voltage protection (UVP) is triggered and shuts down the converter if the output voltage is lower than 50% of its target level. The converter can only be set by POR of V<sub>IN</sub> or toggling the EN pin.

### ***Current Limit Function***

The LTS8002 continuously monitors the inductor current for current limit by sensing the voltage drop across the upper switch when it turns on. When the inductor current is higher than current limit threshold (1.5A typical), the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle.

### ***Thermal Shutdown***

As soon as the junction temperature, T<sub>J</sub>, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, both upper and lower switches are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

## Absolute Maximum Ratings (Note 1)

Input Supply Voltage ( $V_{IN}$ ).....	-0.3V to 6.0V
LX .....	-0.3V to ( $V_{IN} + 0.3V$ ), < 6.0V
Others.....	-0.3V to 6.0V
ESD (Note 2)	
Human Body Mode.....	2kV
Machine Mode.....	200V

## Thermal Information

Continuous Junction Temperature Range .....	-40°C to 150°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 second) .....	260°C
Package Thermal Resistance (Note 3)	
TSOT23-5, $\theta_{JA}$ .....	250°C/W
TSOT23-5, $\theta_{JC}$ .....	25°C/W
TSOT23-6, $\theta_{JA}$ .....	250°C/W
TSOT23-6, $\theta_{JC}$ .....	25°C/W
WDFN2x2-6L, $\theta_{JA}$ .....	135°C/W
WDFN2x2-6L, $\theta_{JC}$ .....	20°C/W
Maximum Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$ (Note 4)	
TSOT23-5 .....	0.4W
TSOT23-6 .....	0.4W
WDFN2x2-6L.....	0.74W

## Recommended Operation Conditions

Continuous Junction Temperature Range .....	-40°C to 120°C
Ambient Temperature Range .....	-40°C to 85°C
Input Voltage Range.....	2.5V to 5.5V

Note 1: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

Note 2: This device is sensitive to electrostatic discharge. Follow proper handling procedures.

Note 3: The Thermal Resistance specifications are based on a JEDEC standard JESD51-3 single-layer PCB.  $\theta_{JA}$  will vary with board size and copper area.

Note 4: The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_{J-MAX}$ , the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any ambient temperature is calculated using:  $P_{D(MAX)} = (T_{J-MAX} - T_A)/\theta_{JA}$ . The maximum power dissipation is determined using  $T_A = 25^\circ\text{C}$ , and  $T_{J-MAX} = 125^\circ\text{C}$ .

## Electrical Characteristics

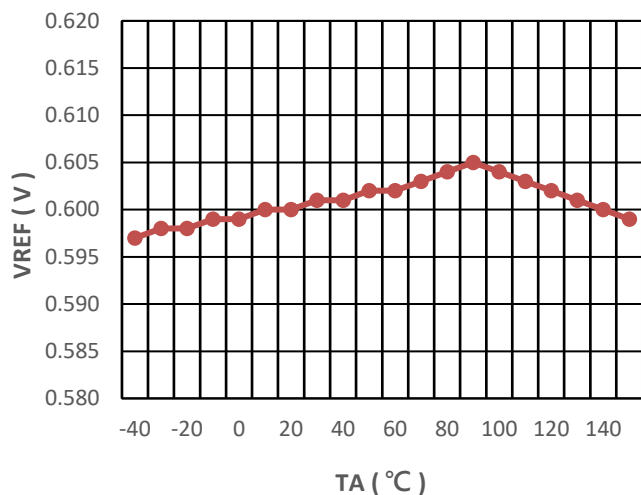
$V_{IN} = V_{EN} = 3.6V$ , and  $T_A = 25^{\circ}C$  unless otherwise specified. External components  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ ,  $L = 2.2\mu H$

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Supply Input</b>						
Supply Input Range	$V_{IN}$		2.5	--	5.5	V
Output Current	$I_{OUT}$		--	--	1.0	A
Shutdown Current	$I_{SD}$	$V_{EN} = 0V$		0.1	1	$\mu A$
Quiescent Current	$I_Q$	$V_{FB} = 0.65V$	--	50	--	$\mu A$
Input Under Voltage Lockout Threshold	$V_{UVLO}$	$V_{IN}$ rising	--	2.3	2.4	V
Input Under Voltage Lockout Hysteresis	$V_{UVHYS}$	$V_{IN}$ falling	--	200	--	mV
<b>Power Switch</b>						
Upper Switch On Resistance	$R_{DS(ON)}$		--	240	--	$m\Omega$
Lower Switch On Resistance			--	180	--	$m\Omega$
Upper Switch Current Limit	$I_{LIM}$		1.2	1.5	--	A
Leakage Current into LX Pin	$I_{LKG}$	$2.5V \leq V_{IN} \leq 5.5V$ , $0V \leq V_{LX} \leq V_{IN}$ , $V_{EN} = 0V$	-1	--	1	$\mu A$
<b>EN</b>						
High Level Input Voltage	$V_{IH}$	$2.5V \leq V_{IN} \leq 5.5V$	1.4	--	$V_{IN}$	V
Low Level Input Voltage	$V_{IL}$	$2.5V \leq V_{IN} \leq 5.5V$	0	--	0.4	V
EN Input Bias Current			-1	--	1	$\mu A$
<b>POK#</b>						
POK# Low Threshold		$V_{FB}$ Rising	--	89	--	% $V_{REV}$
POK# High Threshold		$V_{FB}$ Falling	--	86	--	% $V_{REF}$
POK# Deglitch Time	$t_{DPOK}$	$V_{FB}$ Rising	--	12	--	$\mu s$
<b>Oscillator</b>						
Oscillator Frequency	$f_{OSC}$	$2.5V \leq V_{IN} \leq 5.5V$	1.2	1.5	1.8	MHz
Maximum Duty Cycle		$V_{FB} = 0.55V$ , $V_{IN} = V_{OUT}$	100	--	--	%
<b>Output Voltage</b>						
Adjustable Output Voltage Range	$V_{OUT}$		0.6	--	$V_{IN}$	V
Reference Voltage	$V_{REF}$		590	600	610	mV
Chip Enable Time	$t_{EN}$	Time from active EN to POK# low	--	--	500	$\mu s$
Output Voltage Ramp Up Time	$t_{SS}$	Time to ramp from 5% to 95% of $V_{OUT}$	--	100	--	$\mu s$
Output Under Voltage Threshold	$V_{UV}$	$V_{OUT}$ falling to percent of default value	--	50	--	%
<b>Thermal Shutdown</b>						
Thermal Shutdown Threshold			--	150	--	$^{\circ}C$
Thermal Shutdown Hysteresis			--	20	--	$^{\circ}C$

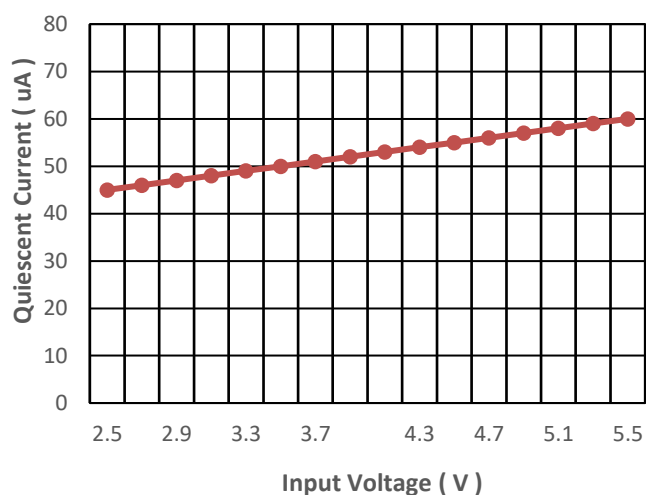


## Typical Characteristic

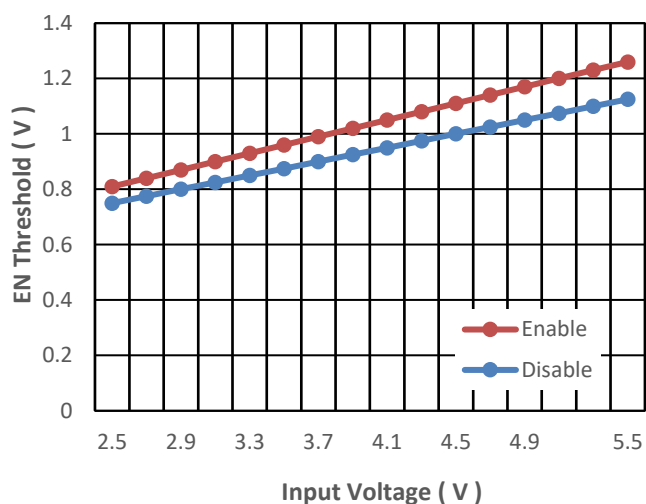
Reference Voltage vs Temperature



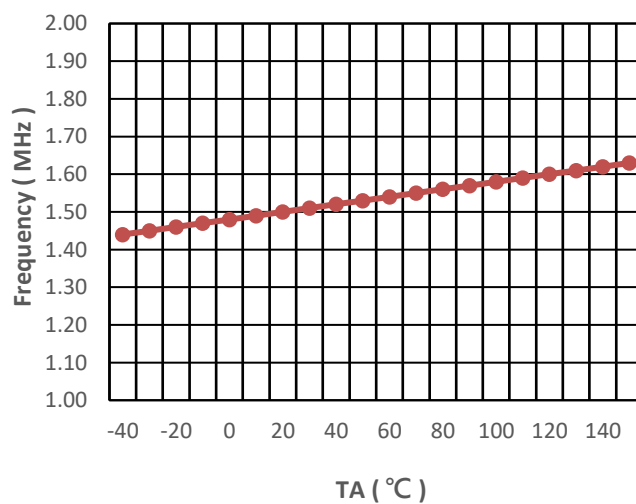
Quiescent Current vs Input Voltage



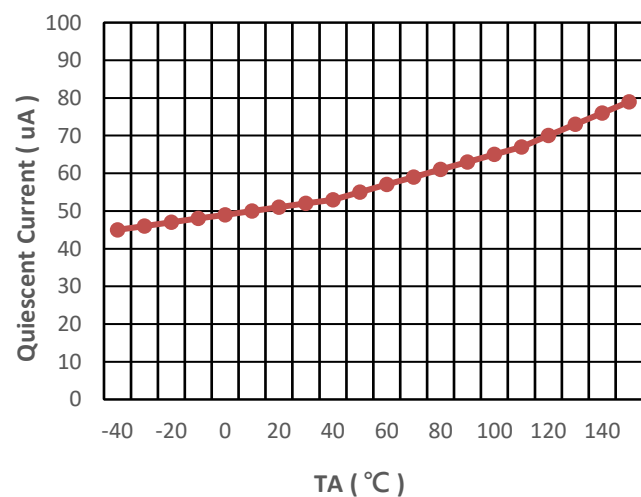
Enable Threshold vs Input Voltage



Charge Current vs Input Voltage



Quiescent Current vs Temperature





## Application Information

### Output Inductor Selection

Output inductor selection is usually based the considerations of inductance, rated current value, size requirements and DC resistance (DCR). The inductance is chosen based on the desired ripple current. Large value inductors result in lower ripple currents and small value inductors result in higher ripple currents.

Higher  $V_{IN}$  or  $V_{OUT}$  also increases the ripple current as shown in the equation below. A reasonable starting point for setting ripple current is  $\Delta I_L = 180\text{mA}$  (30% of 600mA). For most applications, the value of the inductor will fall in the range of 1uH to 10uH.

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current. If possible, choose an inductor with rated current higher than 2.0A so that it will not saturate even under current limit condition.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm-alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends on the price vs. size requirements and any radiated field/EMI requirements.

### Input Capacitance

The LTS8002 draws pulsed current with sharp edges from the input capacitor resulting in ripple and noise at the input supply voltage. A minimum 4.7uF X5R or X7R ceramic capacitor is highly recommended to filter the pulsed current. The input capacitor should be placed as near the device as possible to avoid the stray inductance along the connection trace. Y5V dielectrics, aside from losing most of their capacitance over temperature, they

also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

The capacitor with low ESR (equivalent series resistance) provides the small drop voltage to stabilize the input voltage during the transient loading. For input capacitor selection, the ceramic capacitors larger than 4.7uF is recommend. The capacitor must conform to the RMS current requirement. The maximum RMS ripple current is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at  $V_{IN} = 2 \times V_{OUT}$ , where  $I_{IN(RMS)} = I_{OUT(MAX)}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

### Output Capacitor Selection

The LTS8002 is specifically design to operate with minimum 10uF X5R or X7R ceramic capacitor. The value can be increased to improve load/line transient performance.

The ESR of the output capacitor determines the output ripple voltage and the initial voltage drop following a high slew rate load transient edge. The output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_C \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

where  $f_{OSC}$  = operating frequency,  $C_{OUT}$  = output capacitance and  $\Delta I_C = \Delta I_L$  = ripple current in the inductor.

The ceramic capacitor with low ESR value provides the low output ripple and low size profile. Connect a 10uF ceramic capacitor at output terminal for good performance and place the input and output capacitors as close as possible to the device.

### Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the

presence of other heat-generating components affect the power-dissipation limits of a given component.

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

where  $T_{J(MAX)}$  is the maximum operation junction temperature,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. For recommended operating conditions specification of the LTS8002, The maximum junction temperature is 125°C.

The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. Three basic approaches for enhancing thermal performance are listed below:

- improving the power dissipation capability of the PCB design
- improving the thermal coupling of the component to the PCB by soldering the Exposed Pad.
- introducing airflow in the system

For TSOT23-5 package, the thermal resistance  $\theta_{JA}$  is 250°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula:

$$P_{D(MAX)} = \frac{(125^\circ\text{C} - 25^\circ\text{C})}{250^\circ\text{C/W}} = 0.4\text{W}$$

TSOT23-5 package, the maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ . For LTS8002 package, the Figure 2 of de-rating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

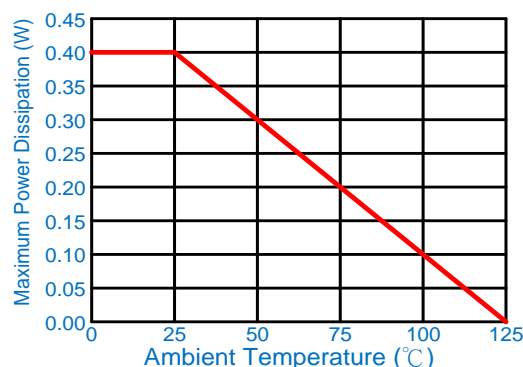


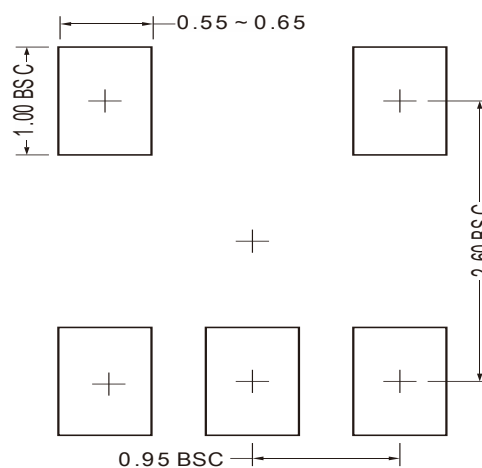
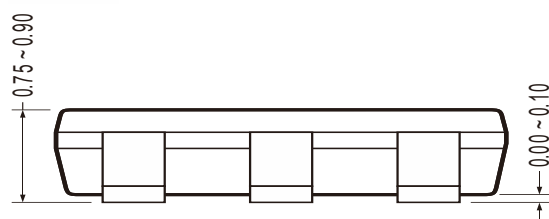
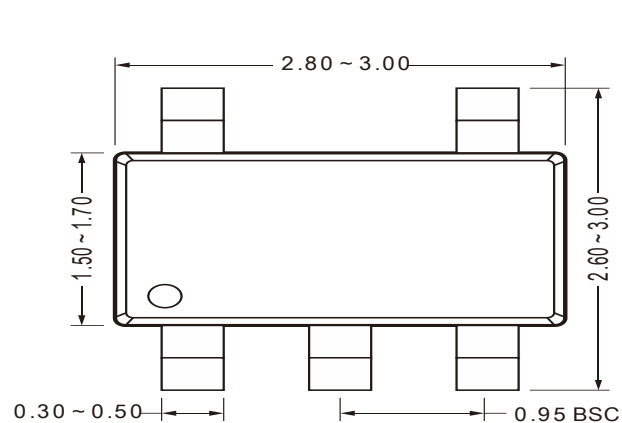
Figure 1: De-rating curve with ambient temperature on the maximum power dissipation allowed.

### PCB Layout Consideration

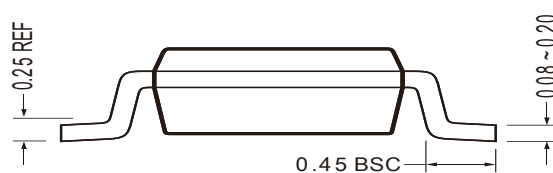
High switching frequencies and relatively large peak currents make the PCB layout a very important part of switching mode power supply design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow the PCB layout guidelines for optimal performance of LTS8002.

1. For the main current paths, keep their traces short, direct and wide. This results in low trace resistance and low parasitic inductance.
2. Put the input/output capacitors as close as possible to the device pins ( $V_{IN}$  and GND).
3. LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
4. Connect feedback network behind the output capacitors. Place the feedback components near the LTS8002 and keep the loop area small.
5. A ground plane is preferred, but if not available, keep the signal and power grounds separated with small signal components returning to the GND pin at one point. They should not share the high current path of  $C_{IN}$  or  $C_{OUT}$ .
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to  $V_{IN}$  or GND.

## Package Information – TSOT23-5

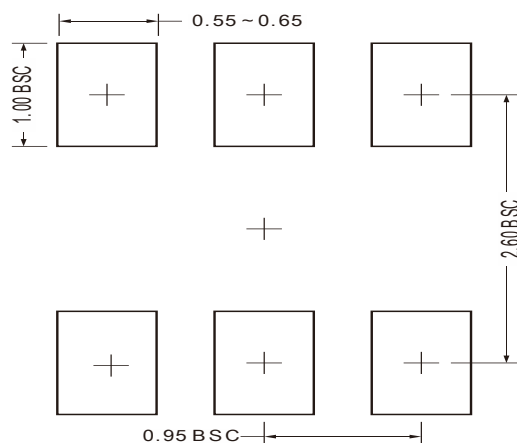
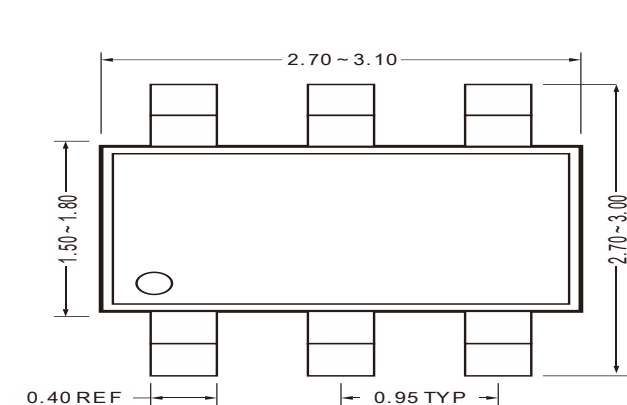


Layout Recommendation

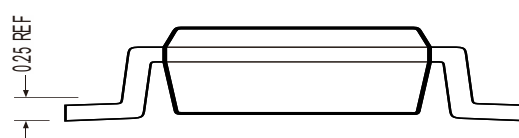
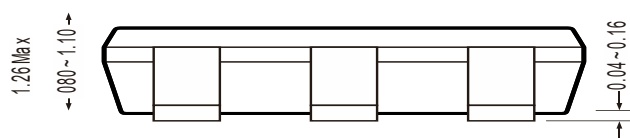


PKG-TSOT236-20120716

## Package Information – TSOT23-6



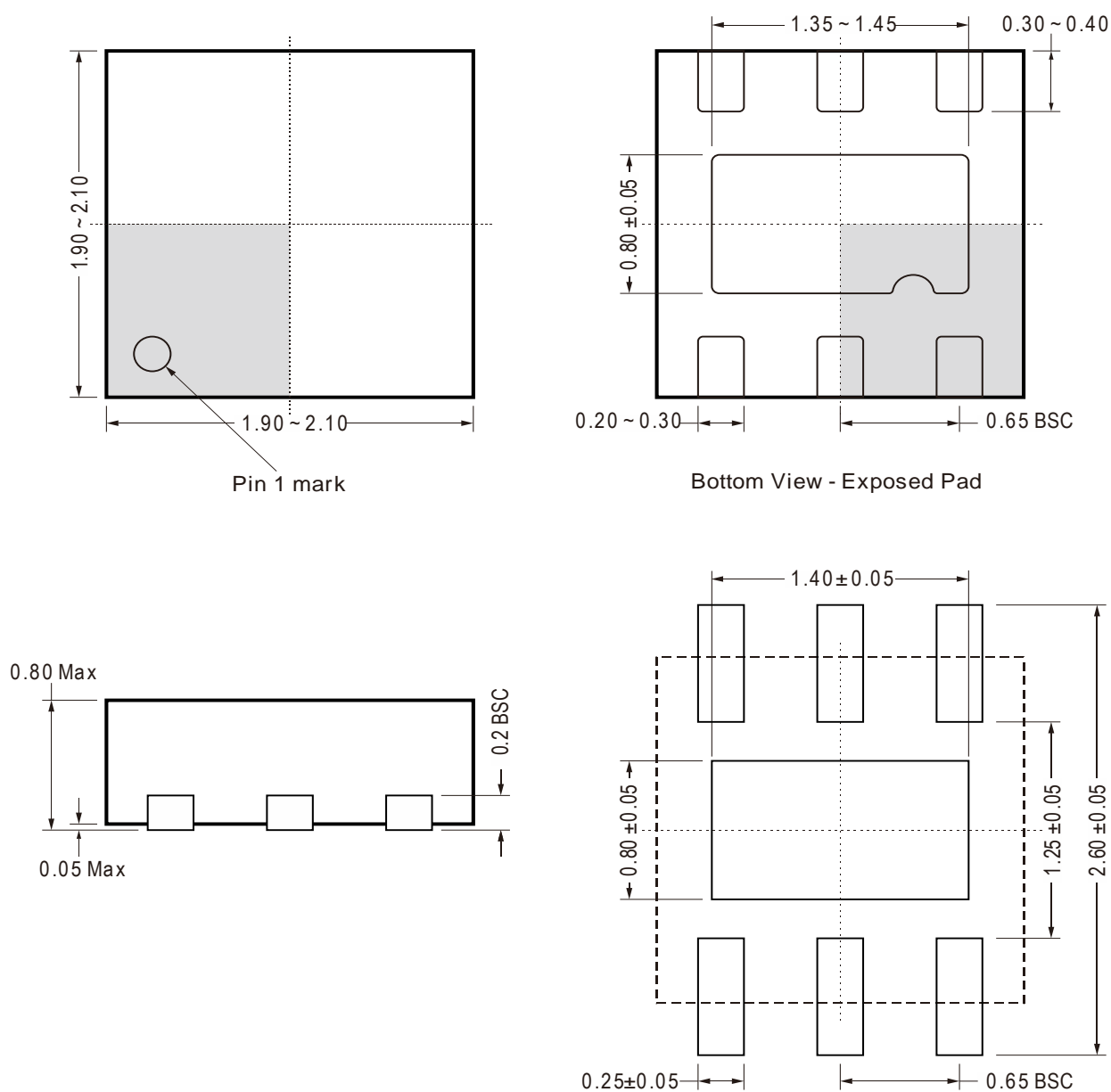
Layout Recommendation



PKG-SOT236-20111208

This package confirms to JDEC MS-012, Variation AA, Issue  
All dimensions are in millimeters.

## Package Information – WDFN2x2-6L



Recommended Solder Pad Pitch and Dimensions

PKG-WDFN2x2-6L-20120706

This package confirms to JEDEC MS-012, Variation AA, Issue  
All dimensions are in millimeters.