80mΩ, 1.5A Power-Distribution Switch With Precision Adjustable Current Limit

General Information

The LTS7602 is a power-distribution switch specifically designed for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered. The device integrates a 80mΩ MOSFET, capable of providing up to 1.5A continuous current. The LTS7602 offers a programmable current-limit threshold between 100mA and 1.5A (typ.) via an external resistor. Current-limit accuracy as tight as ±6% can be achieved at the higher current-limits settings. The devices control output voltage rising and falling slew rate to minimize current surges during turn on/off.

The LTS7602A/B limits the output current to a safe level by using a constant-current mode when the output load exceeds the current threshold. The LTS7602C/D provides circuit breakers functionality by latching off the power switch during overcurrent or reverse-voltage situations.

An internal reverse-voltage comparator disables the power-switch when the output voltage is driven higher than the input to protect devices on the input side of the switch. The FAULT# output asserts low during overcurrent and reverse-voltage conditions. The LTS7602 is available in WDFN2x2-6L and TSOT23-6 packages.

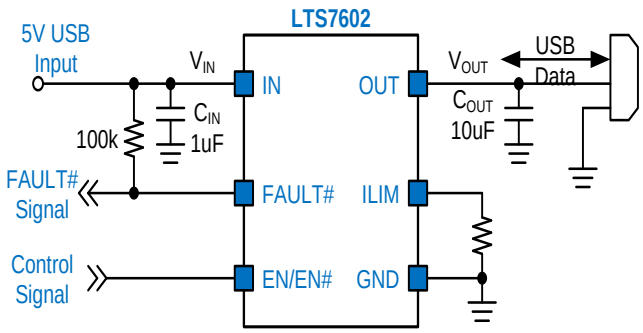
Features

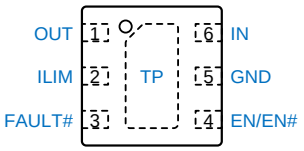
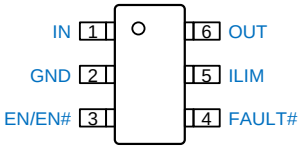
- Up to 1.5A Maximum Load Current
- Typical 100uA Quiescent Current
- ±6% Current-Limit Accuracy at 1.0A
- Meet USB Current-Limiting Requirements
- Adjustable Current Limit, 0.1A ~ 1.5A
- Constant-Current (LTS7602A/B) and Latch-off (LTS7602C/D) Versions
- Fast Current Response – 2us
- 80mΩ High-Side MOSFET
- Reverse Input-Output Voltage Protection
- Operating Range: 2.5V to 5.5V
- Built-In Soft-Start
- RoHS Compliant and Halogen Free

Applications

- USB Bus/Self Powered Hubs
- USB Peripheral Ports
- ACPI Power Distribution
- Battery Powered Equipments
- 3G/3.5G Data Card, Set-Top Boxes

Pin Configuration & Typical Application Circuit



Pin Configuration	Top Marking
 WDFN2X2-6L	 *PPPP: Product Code* *YMDS : Date Code*
 TSOT23-6	 *PPPP: Product Code* *YMDS: Date Code*

Ordering Information

LTS7602□□□□

Version:
A: EN H active, constant current
B: EN# L active, constant current
C: EN H active, latch-off
D: EN# L active, latch-off

Package Type:
ST6: TSOT23-6L
D26: WDFN2x2-6L

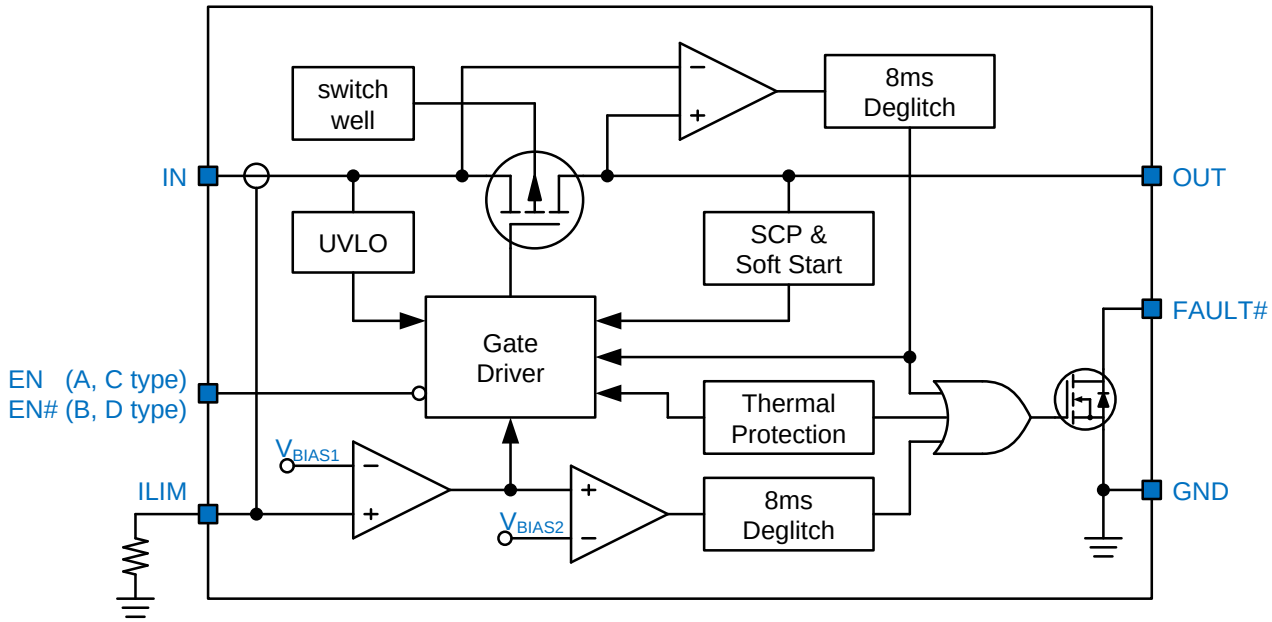
Ordering Number	Package	Top Marking	Note
LTS7602AST6	TSOT23-6	A108	EN High Active, Constant Current
LTS7602AD26	WDFN2x2-6L	A109	
LTS7602BST6	TSOT23-6	A110	EN# Low Active, Constant Current
LTS7602BD26	WDFN2x2-6L	A111	
LTS7602CST6	TSOT23-6	A112	EN High Active, Latch Off
LTS7602CD26	WDFN2x2-6L	A113	
LTS7602DST6	TSOT23-6	A114	EN# Low Active, Latch Off
LTS7602DD26	WDFN2x2-6L	A115	

Leading TECH products are RoHs compliant and compatible with the current requirement of IPC/JDEC J-STD-020 and are suitable for use in SnPb or Pb-Free soldering processes

Functional Pin Descriptions

Pin Number		Pin Name	Description
D26	ST6		
1	6	OUT	**Output Voltage.** This pin is the P-channel MOSFET drain connection. Bypass to ground though a 0.1uF capacitor.
2	5	ILIM	**Current Limit Setting.** Connect an external resistor to set current-limit threshold. Recommended 402Ω < R_{ILIM} < 8.2kΩ.
3	4	FAULT#	**Active Low Open Drain Output.** Asserted during overcurrent, over-temperature, or reverse-voltage conditions.
4	1	IN	**Input Voltage.** This pin is the P-channel MOSFET source connection. Bypass to ground through a 1.0uF capacitor.
5	2	GND	**Ground.** Connect to the thermal pad and to the ground rail of the circuit.
6	3	EN	**Enable Input.** Logic high turns on the power switch. For LTS7602A/C.
		EN#	**Enable Input.** Logic low turns on the power switch. For LTS7602B/D.
Thermal Pad	NA	TP	**Thermal Pad.** Must tie this pad to the ground island/plane through the lowest impedance connection available. This pin is also used as heat-sink of the IC and should be well-soldered to the PCB for optimal thermal performance.

Functional Block Diagram



Operation Principles

The LTS7602 is a current-limited, power- distribution switches using P-channel MOSFET for applications where short circuits or heavy capacitive loads will be encountered. The device allows the users to program the current-limit threshold between 0.1A and 1.5A via an external resistor. Additional device shutdown features include overtemperature protection and reverse-voltage protection. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. There are two device families that handle overcurrent situations differently. The LTS7602A/B family enters constant- current mode while the LTS7602C/D family latches off when the load exceeds the current-limit threshold.

Enable (EN or EN#)

The LTS7602 features a TTL/CMOS compatible EN/EN# pin for enabling/disabling the device. The logic enable controls the power switch, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 1uA when a logic high is present on EN# or when a logic low is present on EN. A logic low input on EN# or a logic high input on EN enables the driver, control circuits, and power switch.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. The UVLO circuit is activated only when the chip is enabled. The UVLO threshold level is typical 2.35V at V_{IN} rising. Built-in 200mV hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

The FAULT# output is set high impedance if V_{IN} is below UVLO threshold.

Slew Rate Control

The LTS7602 control the output voltage slew rate to limit input inrush current when the chip is enabled and UVLO is released. This LTS7602 provides power domain isolation for extended battery life. Three slew rate options, 1us, 100us, and 1ms are available. The LTS7602 integrates a P-Channel MOSFET with typical 80mΩ $R_{DS(ON)}$ delivering up to 1.5A continuous output current.

Overcurrent Conditions

The LTS7602 respond to overcurrent conditions by limiting their output current to the I_{OS} levels shown in Figure 1. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the LTS7602A/B ramps the output current to I_{OS}. The LTS7602A/B devices will limit

the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. The LTS7602C/D devices will limit the current to I_{OS} until the overload condition is removed or the internal deglitch time is reached and the device is turned off. The device will remain off until power is cycled or the device enable is toggled.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS}. The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to I_{OS}. Similar to the previous case, the LTS7602A/B will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle; the LTS7602C/D will limit the current to I_{OS} until the overload condition is removed or the internal deglitch time is reached and the device is latched off.

The LTS7602A/B thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 130℃ while in current limit. The device remains off until the junction temperature cools 20℃ and then restarts. The LTS7602A/B cycles on/off until the overload is removed.

Reverse-Voltage Protection

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV for 8ms. A reverse current of $(V_{OUT} - V_{IN})/R_{DS(ON)}$ will be present when this occurs. This prevents damage to devices on the input side of the LTS7602 by preventing significant current from sinking into the input capacitance. The LTS7602A/B devices allow the N-channel MOSFET to turn on once the output voltage goes below the input voltage for the same 8ms deglitch time. The LTS7602C/D devices keep the device turned off even if the reverse-voltage condition is removed and do not allow the N-channel MOSFET to turn on until power is cycled or the device enable is toggled. The reverse-voltage comparator also asserts the FAULT# output (active-low) after 8ms.

Fault Response

The FAULT# open-drain output is asserted (active low) during an overcurrent, overtemperature or reverse-voltage condition. The LTS7602A/B asserts the FAULT# signal until the fault condition is removed and the device resumes normal operation. The LTS7602C/D asserts the FAULT# signal during a fault condition and remains asserted while the part is latched-off. The FAULT signal is de-asserted once device power is cycled or the enable is toggled and the device resumes normal operation. The LTS7602A/B and LTS7602C/D are designed to eliminate false FAULT# reporting by using an internal delay deglitch circuit for overcurrent and reverse-voltage conditions without the need for external circuitry. This ensures that FAULT# is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the FAULT# signal immediately.

Thermal Protection

The LTS7602A/B and LTS7602C/D have self-protection features using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The LTS7602A/B device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power-switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 130°C and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20 °C. The LTS7602A/B and LTS7602C/D also have a second ambient thermal sensor. The ambient thermal sensor turns off the power-switch when the die temperature exceeds 150°C regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 20 °C. Both the LTS7602A/B and LTS7602C/D families continue to cycle off and on until the fault is removed. The open-drain fault reporting output FAULT# is asserted (active low) immediately during an overtemperature shutdown condition.

Absolute Maximum Ratings (Note 1)

Input Supply Voltage (V_{IN}) ..... -0.3V to 6V

OUT ..... -0.3V to (V_{IN} + 0.3V)

EN/EN# ..... -0.3V to 6V

ESD (Note 2)

Human Body Mode 4kV

Machine Mode 400V

Thermal Information

Continuous Junction Temperature Range ..... -40℃ to 150℃

Storage Temperature Range ..... -65℃ to 150℃

Lead Temperature (Soldering, 10 second) ..... 260℃

Package Thermal Resistance (Note 3)

TSOT23-5, θ_{JA} ..... 250℃/W

TSOT23-5, θ_{JC} ..... 25℃/W

WDFN2x2-6L, θ_{JA} ..... 135℃/W

WDFN2x2-6L, θ_{JC} ..... 20℃/W

Maximum Power Dissipation, P_D @ T_A = 25℃ (Note 4)

TSOT23-5 ..... 0.4W

WDFN2x2-6L 0.74W

Recommended Operation Conditions

Continuous Junction Temperature Range ..... -40℃ to 120℃

Ambient Temperature Range ..... -40℃ to 85℃

Input Voltage Range ..... 2.5V to 5.5V

Note 1: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

Note 2: This device is sensitive to electrostatic discharge. Follow proper handling procedures.

Note 3: The Thermal Resistance specifications are based on a JEDEC standard JESD51-3 single-layer PCB. θ_{JA} will vary with board size and copper area.

Note 4: The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J-MAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{D(MAX)} - T_A)/\theta_{JA}$. The maximum power dissipation is determined using T_A = 25℃, and $T_{J(MAX)}$ = 125℃.

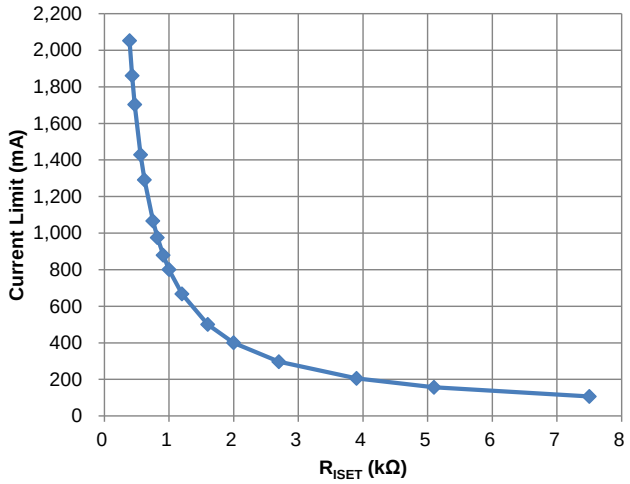
Electrical Characteristics

V_{IN} = 5V, and T_A = 25℃ unless otherwise specified.

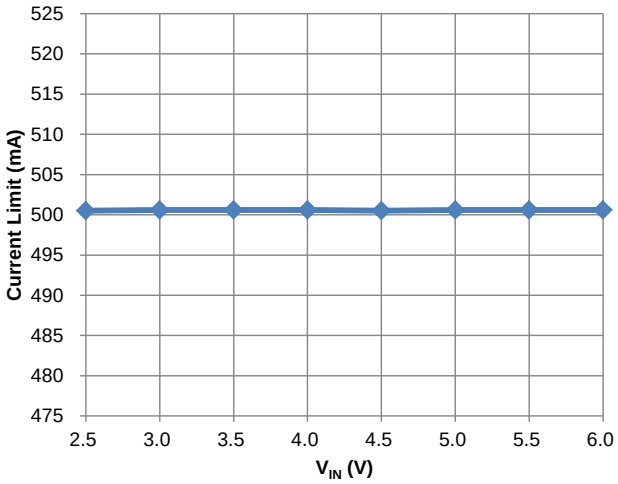
Parameters	Symbol	Condition	Min	Typ.	Max	Unit
Supply Input						
Shutdown Current	I_{SD}	V_{EN} = 0V or $V_{EN\#}$ = 5V		0.1	1	uA
Quiescent Current	I_Q	R_{ILIM} = 1.6kΩ	--	80	120	uA
Reverse Leakage Current	I_{REV}	V_{OUT} = 6V, V_{IN} = 0V	--	0.01	1	uA
Input Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising	--	2.35	2.45	V
Input Undervoltage Lockout Hysteresis	V_{UVHYS}	V_{IN} falling	--	100	--	mV
Reverse-Voltage Comparator Trip Point (V_{OUT} - V_{IN})			95	135	190	mV
Power Switch						
Static Drain-Source On Resistance	$R_{DS(ON)}$	V_{IN} = 5V, I_{OUT} = 50mA	--	80	100	mΩ
Output Rise Time	t_R	V_{IN} = 6V, C_L = 1uF, R_L = 100Ω	--	1.1	1.5	ms
		V_{IN} = 2.5V, C_L = 1uF, R_L = 100Ω	--	0.7	1.0	ms
Output Fall Time	t_F	V_{IN} = 6V, C_L = 1uF, R_L = 100Ω	0.2	--	0.5	ms
		V_{IN} = 2.5V, C_L = 1uF, R_L = 100Ω	0.2	--	0.5	ms
Enable Input EN or EN#						
Enable Pin High Threshold			1.4	--	V_{IN}	V
Enable Pin Low Threshold			0	--	0.4	V
Input Current	I_{EN}	$V_{EN/EN\#}$ = 0V to 6V	-0.5	--	0.5	uA
Turn-on Deglitch Time	t_{ON}	C_L = 1uF, R_L = 100Ω	--	--	3	ms
Turn-off Deglitch Time	t_{OFF}	C_L = 1uF, R_L = 100Ω	--	2	--	us
Current Limit						
Current Limit Threshold, Measured at V_{OUT} = V_{IN} – 0.5V	I_{OS}	R_{ILIM} = 820Ω	917	976	1034	mA
		R_{ILIM} = 1.6kΩ	470	500	530	mA
Response Time to Short Circuit	t_{IOS}		--	2	--	us
FAULT# Flag						
Output Low Voltage	V_{OL}	$I_{FAULT\#}$ = 5mA	0	--	0.2	V
Output High Leakage Current		$V_{FAULT\#}$ = 6V	--	--	1	uA
Fault Deglitch		FAULT# assertion or de-assertion due to overcurrent condition	4	8	12	ms
		FAULT# assertion or de-assertion due to reverse-voltage condition	4	8	12	ms
Thermal Shutdown						
Thermal Shutdown Threshold			--	150	--	℃
Thermal Shutdown Hysteresis				20		℃

Typical Characteristics

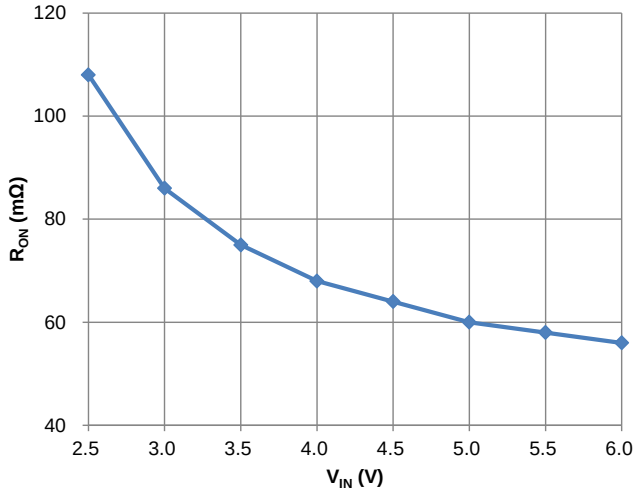
Current Limit vs ILIM Resistor



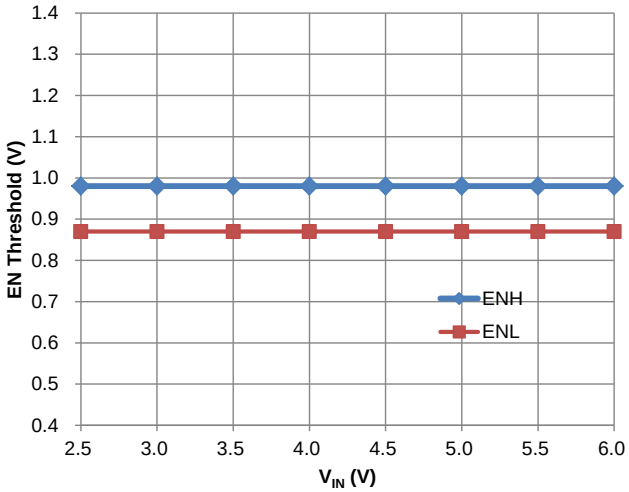
Current Limit vs Input Voltage



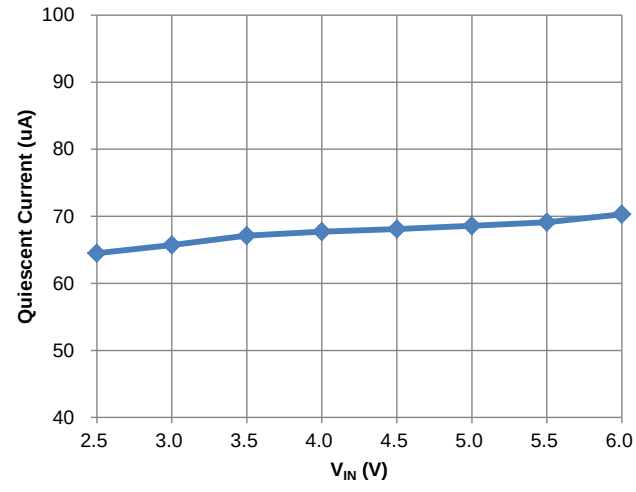
R_{ON} vs Input Voltage



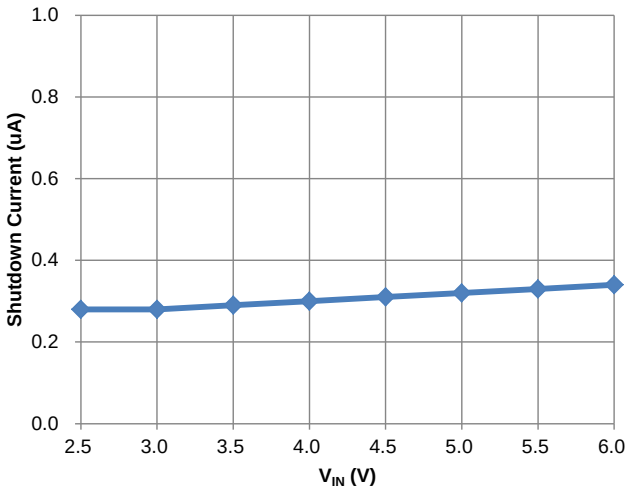
EN Threshold vs Input Voltage



Input Quiescent Current vs Input Voltage



Input Shutdown Current vs Input Voltage



Application Information

Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1uF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The LTS7602A/B and LTS7602C/D use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 402Ω < R_{ILIM} < 8.2kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations and Figure 1-1 & 1-2 can be used to calculate the resulting overcurrent threshold for a given external resistor value (R_{ILIM}). Figure 1-1 & 1-2 includes current-limit tolerance due to variations caused by temperature and process.

However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting R_{ILIM}. The traces routing the R_{ILIM} resistor to the LTS7602A/B and LTS7602C/D should be as short as possible to reduce parasitic effects on the current-limit accuracy.

Current-Limit Threshold Equations (I_{OS}):

$$I_{OS,TYP}\,(mA) = 800(V)/R_{ILIM}(k\Omega)$$

where 402Ω < R_{ILIM} < 8.2kΩ.While the maximum recommended value of R_{ILIM} is 8.2kΩ, there is one additional configuration that allows for a lower current-limit threshold. The ILIM pin may be connected directly to IN to provide a 98mA current-limit threshold.

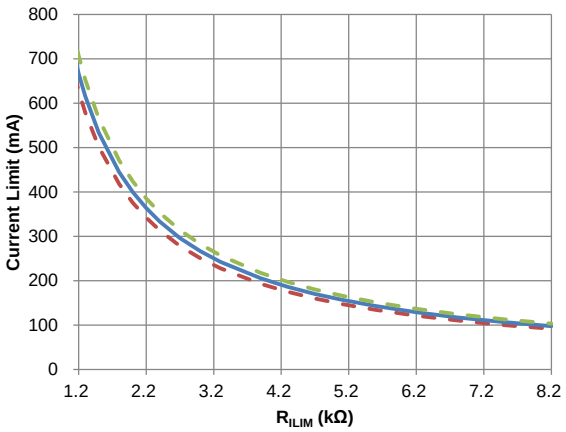


Figure 1-1. Current Limit Threshold vs. R_{ILIM}

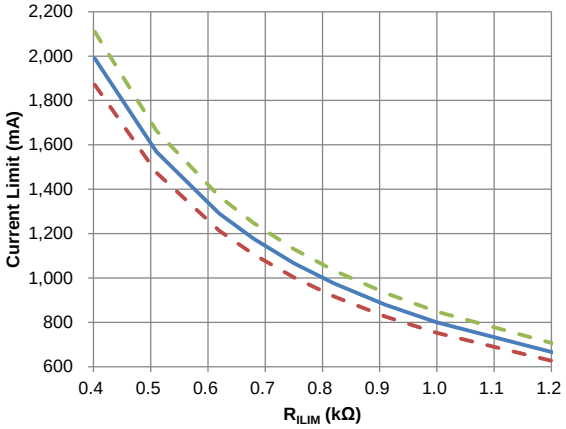


Figure 1-2. Current Limit Threshold vs. R_{ILIM}

Accounting for Resistor Tolerance

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the LTS7602A/B and LTS7602C/D performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired.

Table 1. **Common R_{ILIM} Resistor Selections**

1% Resistor	Resistor Tolerance		Actual Limits		
	1% low	1% high	$I_{OS,MIN}$ (mA)	I_{OS} (mA)	$I_{OS,MAX}$ (mA)
8.06 kΩ	7.979 kΩ	8.141 kΩ	98.3	99.3	100.3
4.02 kΩ	3.980 kΩ	4.060 kΩ	197.0	199.0	201.0
2.67 kΩ	2.643 kΩ	2.697 kΩ	296.7	299.6	302.7
2 kΩ	1.980 kΩ	2.020 kΩ	396.0	400.0	404.0
1.6 kΩ	1.584 kΩ	1.616 kΩ	495.0	500.0	505.1
1.33 kΩ	1.377 kΩ	1.343 kΩ	595.5	601.5	607.6
1.15 kΩ	1.139 kΩ	1.162 kΩ	688.8	695.7	702.7
1 kΩ	0.990 kΩ	1.010 kΩ	792.1	800.0	808.1
887 Ω	878.13 Ω	895.87 Ω	893.0	901.9	911.0
806 Ω	797.94 Ω	814.06 Ω	982.7	992.6	1002.6
727 Ω	719.73 Ω	734.27 Ω	1089.5	1092.9	1111.5
665 Ω	658.35 Ω	671.65 Ω	1191.1	1203.0	1215.2
619 Ω	612.81 Ω	625.19 Ω	1279.6	1292.4	1305.5
576 Ω	570.24 Ω	581.76 Ω	1375.1	1388.9	1402.9
536 Ω	530.64 Ω	541.36 Ω	1477.8	1492.5	1507.6

Constant-Current vs. Latch-Off Operation and Impact on Output Voltage

Both the constant-current devices (LTS7602A/B) and latch-off devices (LTS7602C/D) operate identically during normal operation, i.e. the load current is less than the current-limit threshold and the devices are not limiting current. During normal operation the P-channel MOSFET is fully enhanced, and $V_{OUT} = V_{IN} - (I_{OUT} \times R_{DS(ON)})$. The voltage drop across the MOSFET is relatively small compared to V_{IN}, and $V_{OUT} \approx V_{IN}$.

Both the constant-current devices LTS7602A/B and latch-off devices LTS7602C/D operate identically during the initial onset of an overcurrent event. Both devices limit current to the programmed current-limit threshold set by R_{ILIM} by operating the P-channel MOSFET in the linear mode. During current-limit operation, the P-channel MOSFET is no longer fully-enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{OUT} \neq V_{IN}$), and V_{OUT} decreases.

While both the constant-current devices LTS7602A/B and latch-off devices LTS7602C/D operate identically during the initial onset of an overcurrent event, they behave differently if the overcurrent event lasts longer than the internal delay deglitch circuit. The constant-current devices assert the FAULT# flag after the deglitch period and continue to regulate the current to the current-limit threshold indefinitely. In practical circuits, the power dissipation in the package will increase the die temperature above the over-temperature shutdown threshold (130℃), and the device will turn off until the die temperature decreases by the hysteresis of the thermal shutdown circuit (20℃). The device will turn on and continue to thermal cycle until the overload condition is removed. The constant-current devices resume normal operation once the overload condition is removed. The latch-off devices LTS7602C/D assert the FAULT# flag after the deglitch period and immediately turn off the device. The device remains off regardless of whether the overload condition is removed from the output. The latch-off devices remain off and do not resume normal operation until the surrounding system either toggles the enable or cycles power to the device.

Power Dissipation and Junction Temperature

The low on-resistance of the P-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $R_{DS(ON)}$ of the P-channel

MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $R_{DS(ON)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$P_D = R_{DS(ON)} \times I_{OUT}^2$

where:

P_D = Total power dissipation (W)

$R_{DS(ON)}$ = Power switch on-resistance ()

I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the P-channel MOSFET.

Finally, calculate the junction temperature:

$T_J = P_D \times \theta_{JA} + T_A$

where:

T_A = Ambient temperature (℃)

θ_{JA} = Thermal resistance (℃/W)

P_D = Total power dissipation (W)

The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout.

Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, FAULT# pulls low disabling the part. The part is disabled when EN is pulled low, and FAULT# goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on EN reaches the turn on threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

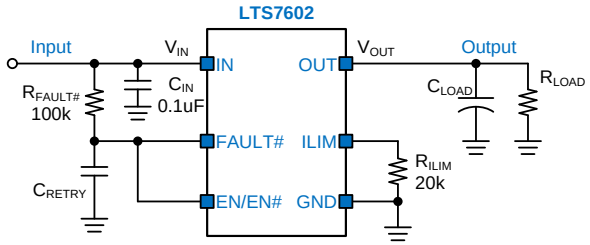


Figure 2. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal.

The figure below shows how an external logic signal can drive EN through RFAULT# and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

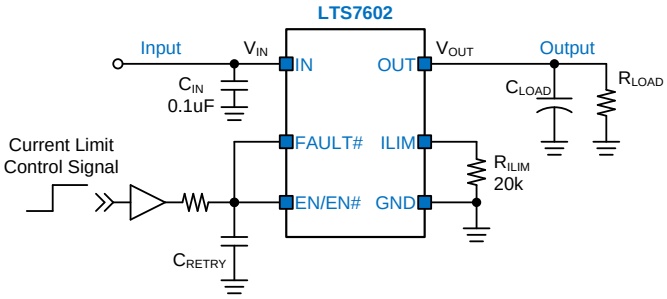


Figure 3. Auto-Retry Function with External EN Signal.

Two Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. Figure 4 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND. A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

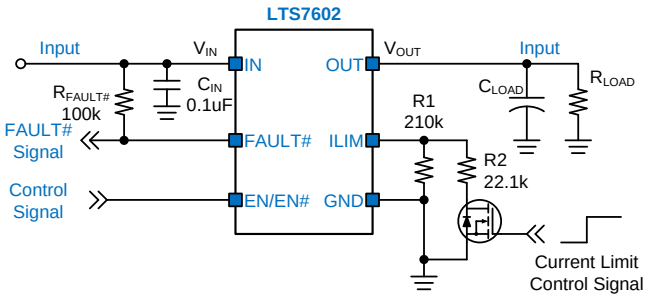
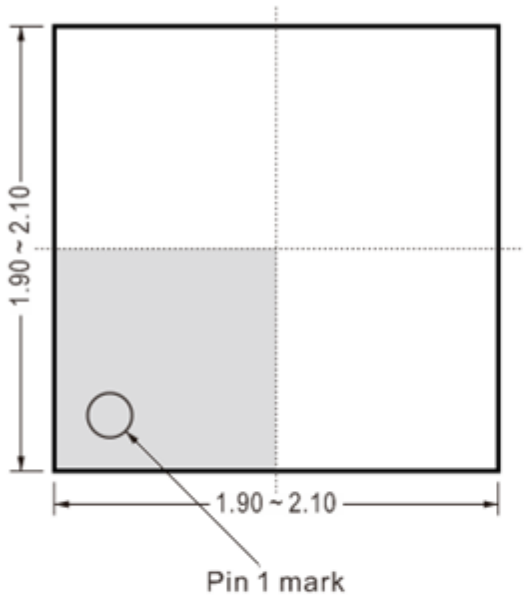
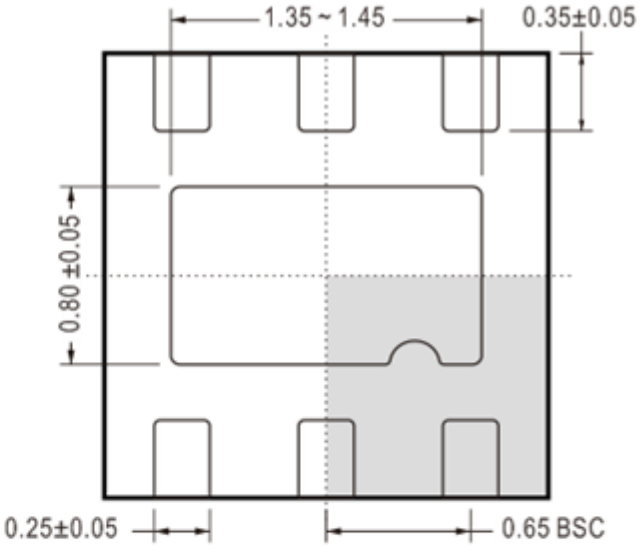


Figure 4. Two Level Current Limit Circuit.

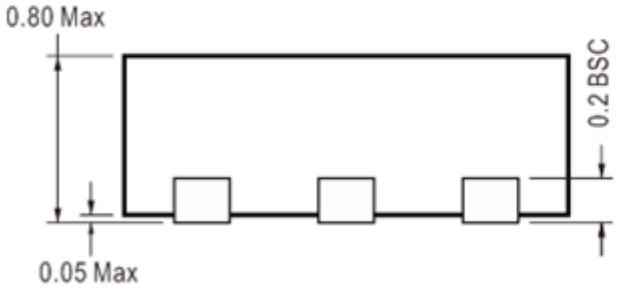
Package Information – WDFN2x2-6L

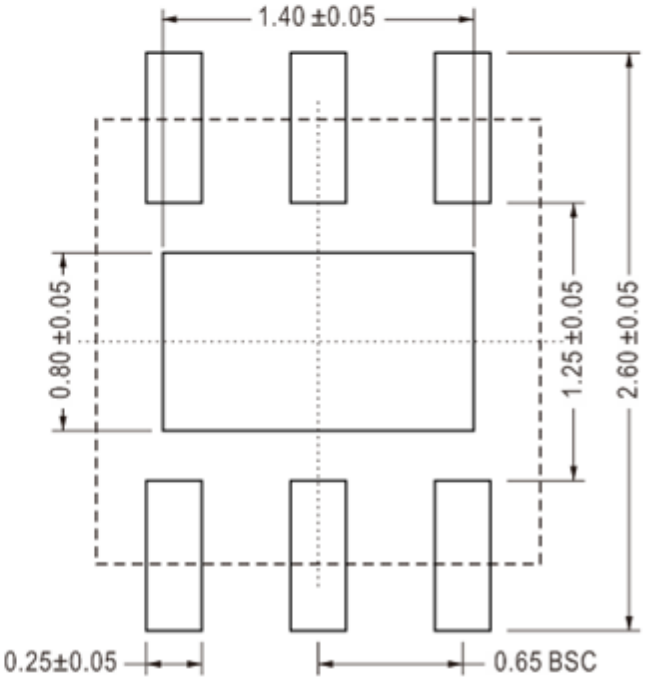
Unit: mm.





Bottom View - Exposed Pad





Recommended Solder Pad Pitch and Dimensions

Package Information – TSOT23-6