Low Noise, High PSRR 700mΩ LDO Regulator

General Information

The LTS7001 is a high performance LDO regulator specifically designed to deliver fixed/adjustable output voltage with high PSRR and fast transient response. Internal 700mohm PMOS pass transistor yields typical 420mV dropout voltage at 600mA output current.

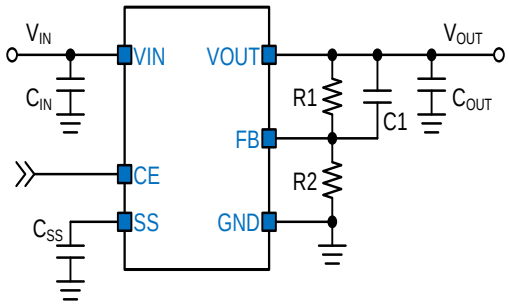
Typical quiescent current is only 65uA. A logic low on the enable input, CE, shuts down the output and reduces the supply current to less than 1uA. The LTS7001 works stably with as low as 1uF ceramic output capacitor, minimizing board space requirement.

Other features include adjustable soft start, high output accuracy, output current limiting, and thermal protection. The LTS7001 is available in the TSOT23-5, TSOT23-6, or WDFN1.6x1.6 packages.

Applications

- Battery-Powered Equipment's
- Hand-Held Electrical Appliances
- Portable Communication Equipment's

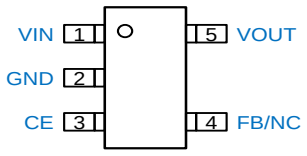
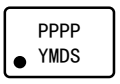
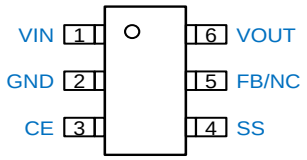
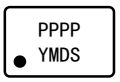
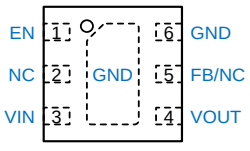
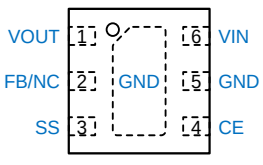
Typical Applications Circuit



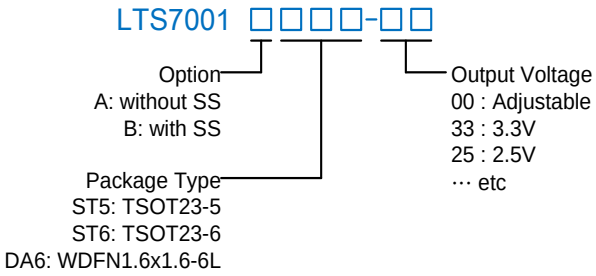
Features

- **Wide Input Voltage Range, 2.2V to 6.0V**
- **Fixed or Adjustable Output Voltage**
- **High Output Voltage Accuracy, +/-1%**
- **Fast Transient Response**
- **Typical 420mV Dropout Voltage at 600mA Output Current**
- **Small Output Capacitor, 1uF**
- **Typical 65uA Quiescent Current**
- **Less Than 1uA Shutdown Current**
- **Dedicated Chip Enable Pin**
- **Fixed or Adjustable Soft Start**
- **Over Current Limitation**
- **Thermal Protection**
- **TSOT23-5, TSOT23-6, WDFN1.6x1.6 Packages**
- **RoHS Compliant and Halogen Free**

Pin Configuration & Top Marking

Pin Configuration	Top Marking
 TSOT23-5	 *PPPP: Product Code* *YMDS : Date Code*
 TSOT23-6	 *PPPP: Product Code* *YMDS: Date Code*
 WDFN1.6x1.6-6L	 *PPPP: Product Code* *YMDS: Date Code*
 WDFN1.6x1.6-6L	 *PPPP: Product Code* *YMDS: Date Code*

Ordering Information



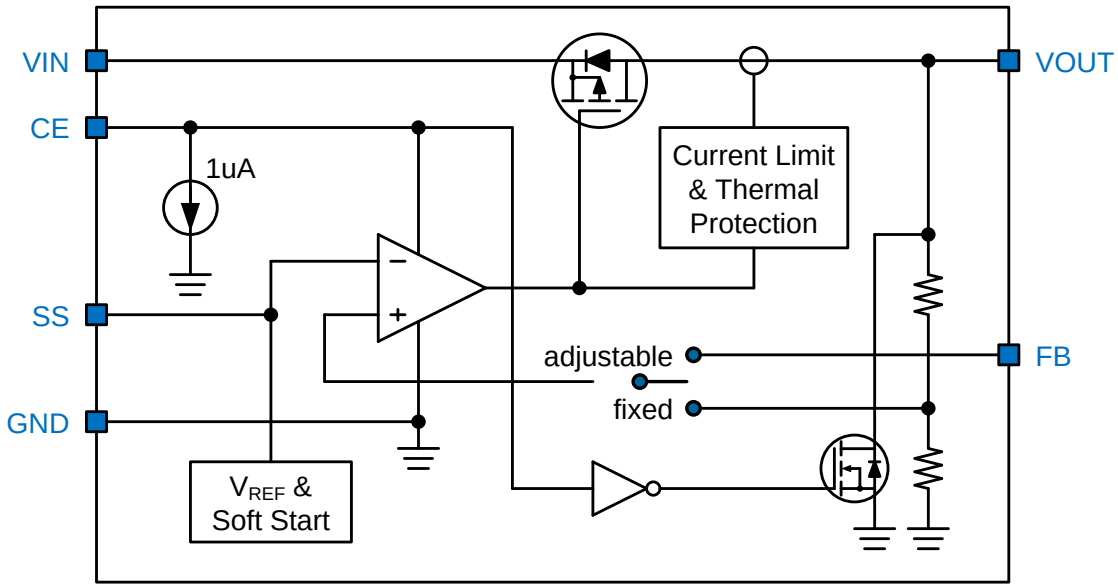
Ordering Number	Package	Top Marking (Product Code)	Note
LTS7001AST5 - 00	TSOT23-5	A007	Adjustable Output Voltage
LTS7001AST5 - 33	TSOT23-5	A008	3.3V Output Voltage
LTS7001AST5 - 30	TSOT23-5	A009	3.0V Output Voltage
LTS7001AST5 - 28	TSOT23-5	A011	2.8V Output Voltage
LTS7001AST5 - 25	TSOT23-5	A013	2.5V Output Voltage
LTS7001AST5 - 18	TSOT23-5	A010	1.8V Output Voltage
LTS7001AST5 - 15	TSOT23-5	A015	1.5V Output Voltage
LTS7001AST5 - 12	TSOT23-5	A016	1.2V Output Voltage
LTS7001AST5 - 10	TSOT23-5	A040	1.0V Output Voltage
LTS7001ADA6 - 00	WDFN1.6x1.6-6L	A017	Adjustable Output Voltage
LTS7001ADA6 - 33	WDFN1.6x1.6-6L	A018	3.3V Output Voltage
LTS7001ADA6 - 30	WDFN1.6x1.6-6L	A019	3.0V Output Voltage
LTS7001ADA6 - 28	WDFN1.6x1.6-6L	A020	2.8V Output Voltage
LTS7001ADA6 - 25	WDFN1.6x1.6-6L	A021	2.5V Output Voltage
LTS7001ADA6 - 18	WDFN1.6x1.6-6L	A014	1.8V Output Voltage
LTS7001ADA6 - 15	WDFN1.6x1.6-6L	A022	1.5V Output Voltage
LTS7001ADA6 - 12	WDFN1.6x1.6-6L	A023	1.2V Output Voltage
LTS7001BST6 - 00	TSOT23-6	A012	Adjustable Output Voltage
LTS7001BST6 - 33	TSOT23-6	A025	3.3V Output Voltage
LTS7001BST6 - 30	TSOT23-6	A026	3.0V Output Voltage
LTS7001BST6 - 28	TSOT23-6	A027	2.8V Output Voltage
LTS7001BST6 - 25	TSOT23-6	A028	2.5V Output Voltage
LTS7001BST6 - 18	TSOT23-6	A029	1.8V Output Voltage
LTS7001BST6 - 15	TSOT23-6	A030	1.5V Output Voltage
LTS7001BST6 - 12	TSOT23-6	A031	1.2V Output Voltage
LTS7001BDA6 - 00	WDFN1.6x1.6-6L	A032	Adjustable Output Voltage
LTS7001BDA6 - 33	WDFN1.6x1.6-6L	A033	3.3V Output Voltage
LTS7001BDA6 - 30	WDFN1.6x1.6-6L	A034	3.0V Output Voltage
LTS7001BDA6 - 28	WDFN1.6x1.6-6L	A035	2.8V Output Voltage
LTS7001BDA6 - 25	WDFN1.6x1.6-6L	A036	2.5V Output Voltage
LTS7001BDA6 - 18	WDFN1.6x1.6-6L	A037	1.8V Output Voltage
LTS7001BDA6 - 15	WDFN1.6x1.6-6L	A038	1.5V Output Voltage
LTS7001BDA6 - 12	WDFN1.6x1.6-6L	A039	1.2V Output Voltage

Note 1. Leading TECH products are RoHs compliant and compatible with the current requirement of IPC/JDEC J-STD-020 and are suitable for use in SnPb or Pb-Free soldering processes.

Functional Pin Descriptions

Pin Name	Pin Function
VIN	**Input Voltage**. Connect a minimum 1uF ceramic capacitor to this pin for stable operation.
GND	**Ground**.
EN	**Active High Chip Enable**. This pin is internally pulled down by a 1uA current source.
FB/NC	**Output Voltage Feedback**. Available only for adjustable output voltage version. The FB voltage is regulated to 0.8V. Connect a resistive voltage divider to set the output voltage.
VOUT	**Output Voltage**. Connect a minimum 1uF ceramic capacitor to this pin for stable operation.
SS	**Soft Start.** Connect a 1nF ~ 10nF ceramic capacitor to set soft start time.

Functional Block Diagram



Operation Principles

The LTS7001 low dropout regulator (LDO) operates with a very low input voltage (>2.2V). The LTS7001 can operate at low input voltage due to low voltage circuit design techniques and a PMOS pass element that exhibits low dropout. The dropout voltage is typically 420mV at 600mA output current.

Chip Enable

Typical quiescent current is only 65uA. A logic low on the enable input, CE, shuts down the output and reduces the supply current to less than 1uA. The CE pin is internally pulled down by a 1uA current source and may be tied to VIN in applications where the shutdown feature is not used.

Output Discharging Resistor

An internal 100Ω MOSFET is connected to VOUT pin and discharges the output voltage to ground when the chip is disabled or thermal protection is triggered.

Soft Start

The LTS7001 features adjustable soft start where SS pin is available. A 8uA current source charges the soft start capacitor C_{SS} and clamps output voltage ramping up speed. The soft start time is calculated as:

$$T_{SS} = C_{SS} \times \frac{0.8V}{8uA}$$

A 1nF yields 100ns soft start time. The soft start time is fixed as 100us where SS pin is not available.

Output Voltage Programming

The output voltage of the LTS7001 adjustable regulator is programmed using an external resistive divider as shown in the typical application circuit. The output voltage is calculated as:

$$V_{OUT} = V_{REF} \times \frac{R1 + R2}{R2}$$

where V_{REF} = 0.8V typ (the internal reference voltage.)

Resistors R1 and R2 should be chosen for approximately 10uA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error.

Current Limit and Thermal Protection

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 800mA. Further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 160^{O}C. Recovery is automatic when the junction temperature drops approximately 30^{O}C below the high temperature trip point.

Pass Element

The LTS7001 integrates a 700mΩ PMOS pass element that enables very low dropout voltage. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

Absolute Maximum Ratings (Note 1)

Input Supply Voltage (V_{IN}) ..... -0.3V to 6.5V
Voltage at EN ..... -0.3V to 6.5V
Others ..... -0.3V to (V_{IN} + 0.3V)
ESD (Note 2)
- Human Body Mode 2kV
- Machine Mode 200V

Thermal Information

Continuous Junction Temperature Range ..... -40°C to 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 second) ..... 260°C
Package Thermal Resistance (Note 3)
- TSOT23-5, θ_{JA} ..... 250°C/W
- TSOT23-5, θ_{JC} ..... 25°C/W
- TSOT23-6, θ_{JA} ..... 250°C/W
- TSOT23-6, θ_{JC} ..... 25°C/W
- WDFN1.6x1.6-6L, θ_{JA} ..... 150°C/W
- WDFN1.6x1.6-6L, θ_{JC} ..... 30°C/W

Maximum Power Dissipation, P_D @ T_A = 25°C (Note 4)
- TSOT23-5 ..... 0.4W
- TSOT23-6 ..... 0.4W
- WDFN1.6x1.6-6L 0.67W

Recommended Operation Conditions

Continuous Junction Temperature Range ..... -40°C to 125°C
Ambient Temperature Range ..... -40°C to 85°C
Input Voltage Range ..... 2.2V to 6.0V

Note 1: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

Note 2: This device is sensitive to electrostatic discharge. Follow proper handling procedures.

Note 3: The Thermal Resistance specifications are based on a JEDEC standard JESD51-3 single-layer PCB. θ_{JA} will vary with board size and copper area.

Note 4: The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J-MAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{D(MAX)} - T_A)/\theta_{JA}$. The maximum power dissipation is determined using T_A = 25°C, and $T_{J(MAX)}$ = 125°C.

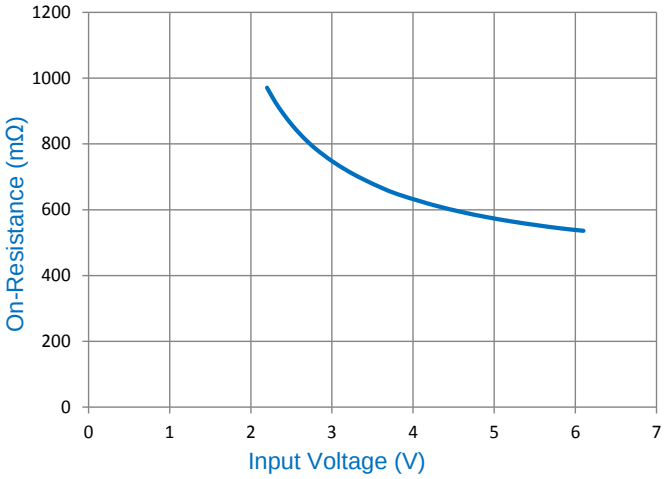
Electrical Characteristics

V_{IN} = V_{EN} = 3.3V and T_A = 25°C unless otherwise specified.

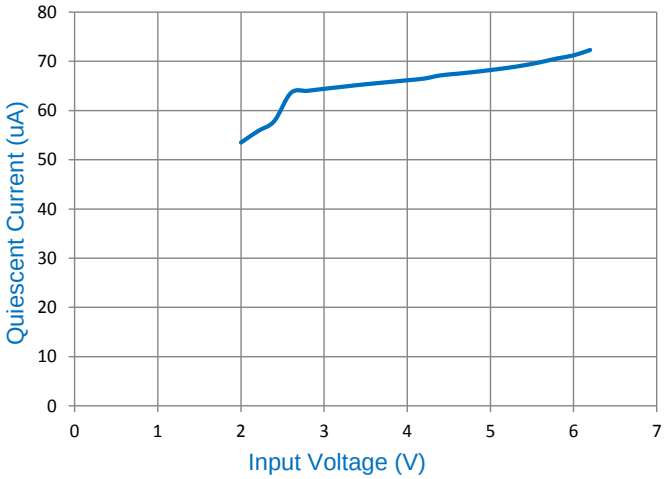
Parameters	Symbol	Condition	Min	Typ	Max	Unit
Input Supply Voltage	V_{IN}		2.2	--	6.0	V
V_{IN} Under Voltage Lockout	V_{UVLO}		--	2	2.1	V
Shutdown Current	I_{SD}	V_{EN} = 0V	--	--	1	uA
Quiescent Current	I_Q	I_{OUT} = 0mA	--	65	--	uA
Output Voltage Accuracy	V_{OUT}	Fixed Output Voltage, I_{OUT} = 10mA	-1	--	1	%
FB Pin Voltage	V_{FB}	Adjustable Version, I_{OUT} = 10mA	792	800	808	mV
Maximum Output Current	I_{OUT}		600	800	--	mA
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	1mA < I_{OUT} < 600mA	--	30	50	mV
On-Resistance of Pass Element	$R_{DS(ON)}$		--	700	--	mΩ
Dropout Voltage	V_{DP}	I_{OUT} = 600mA	--	420	--	mV
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 0.42V < V_{IN} < 6.0V	--	0.02	--	%/V
Output Noise		BW = 10Hz to 100kHz, I_{OUT} = 10mA	--	70	--	uVrms
Power Supply Ripple Rejection	PSRR	I_{OUT} = 10mA, f = 1kHz	--	-70	--	dB
		I_{OUT} = 10mA, f = 10kHz	--	-60	--	dB
Short Circuit Limit		V_{OUT} = 0V	--	100	--	mA
EN Pull-Down Constant Current	I_{EN}	V_{EN} = 3.3V	--	1	--	uA
EN Input High Threshold	V_{IH}		1.6	--	--	V
EN Input Low Threshold	V_{IL}		--	--	0.4	V
Soft Start Time	t_{SS}	fixed version,	--	100	--	uS
SS Pin Sourcing Current	I_{SS}	V_{SS} = 0V	--	8.0	--	uA
Thermal Shutdown Temperature	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	30	--	°C

Typical Characteristics

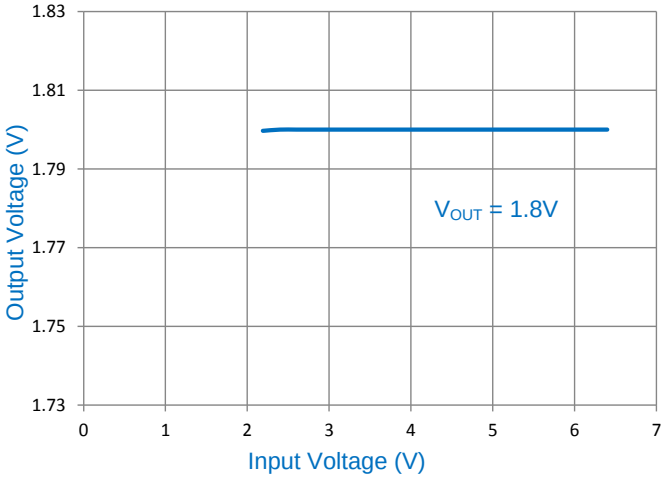
On-Resistance vs. Input Voltage



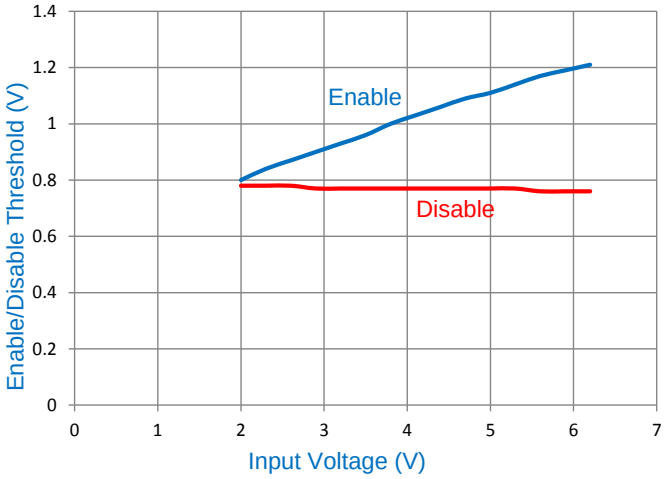
Quiescent Current vs. Input Voltage



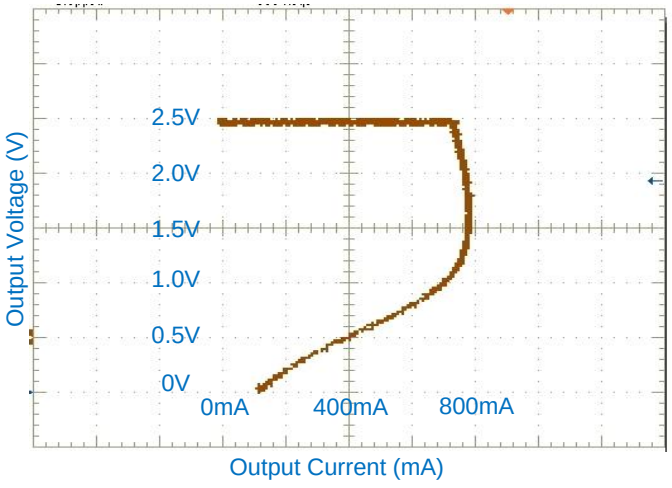
Line Regulation



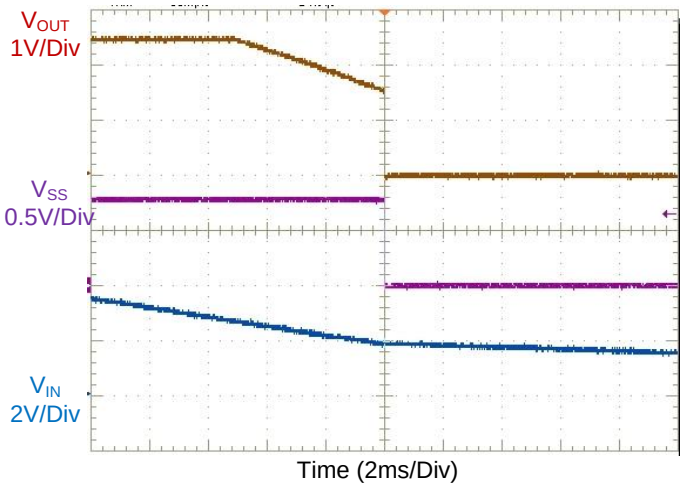
Enable Disable Threshold vs. Input Voltage



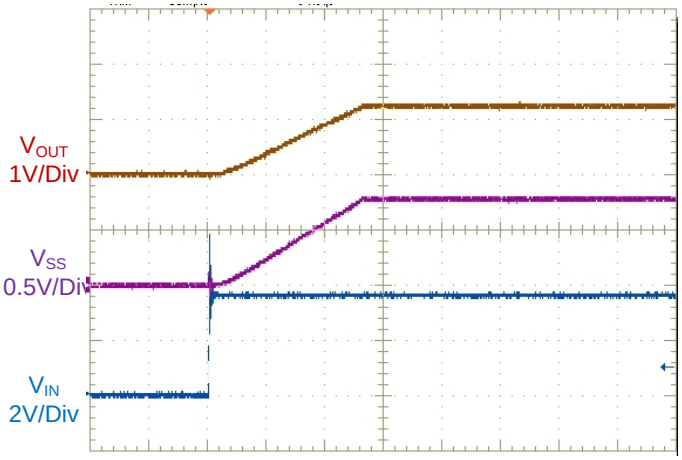
Output Current Limit



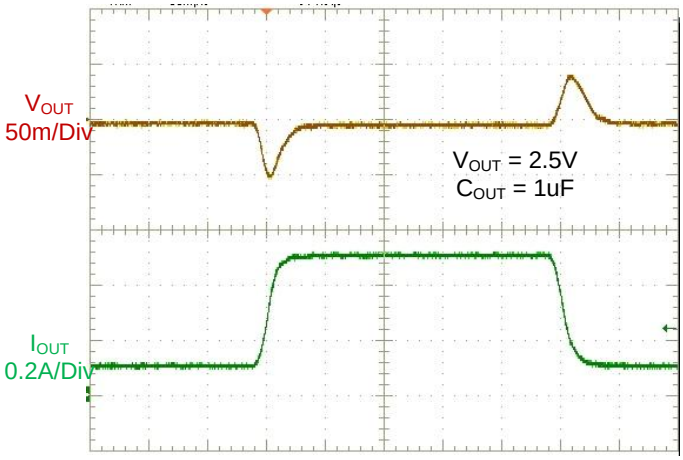
Power Off Waveforms



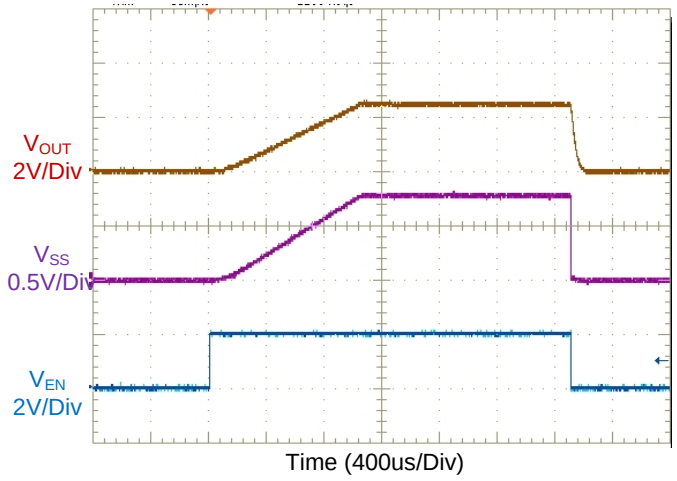
Power On Waveforms



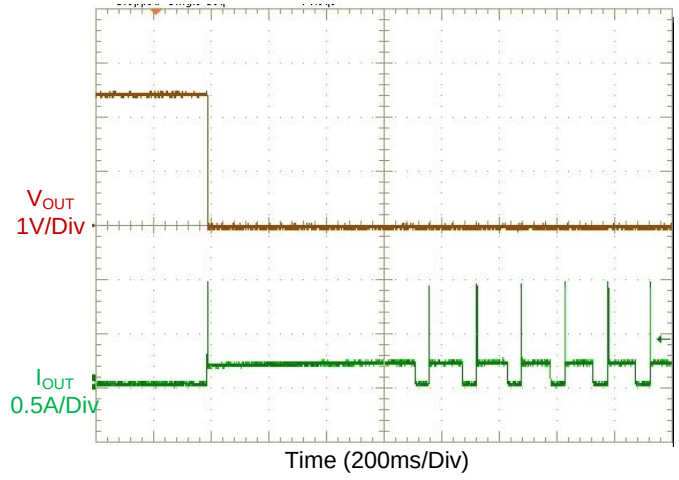
Load Transient Response



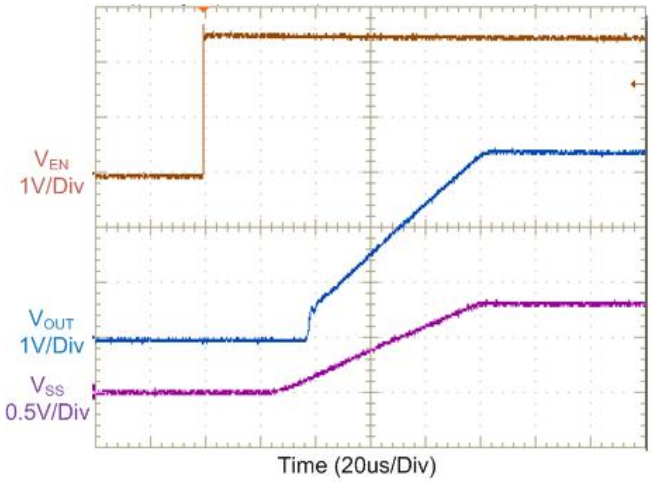
Turn On/Off Waveforms



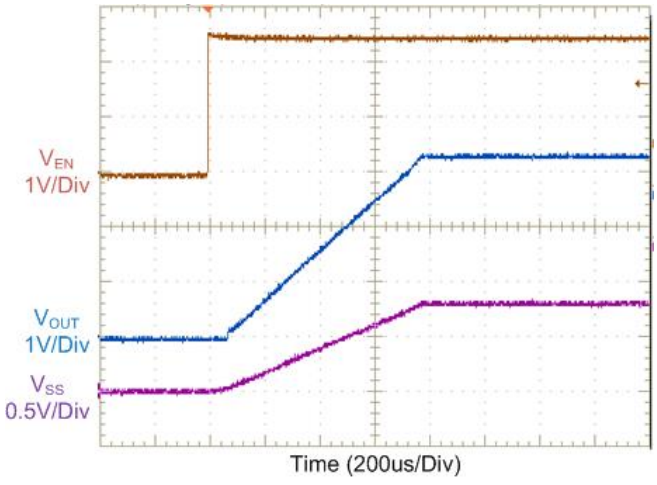
Output Short Circuit Response



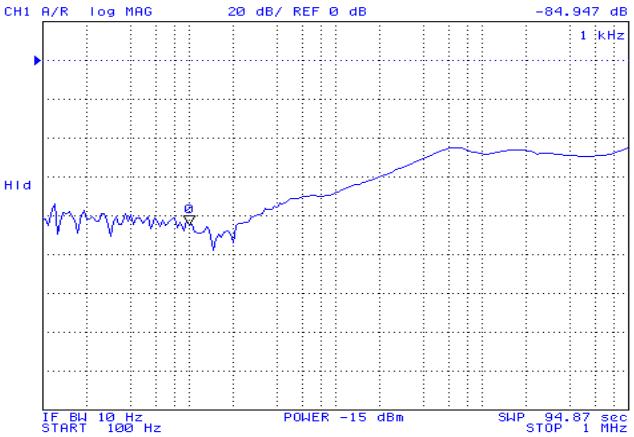
Soft Star Time (1nF) Waveforms



Soft Star Time (10nF) Waveforms

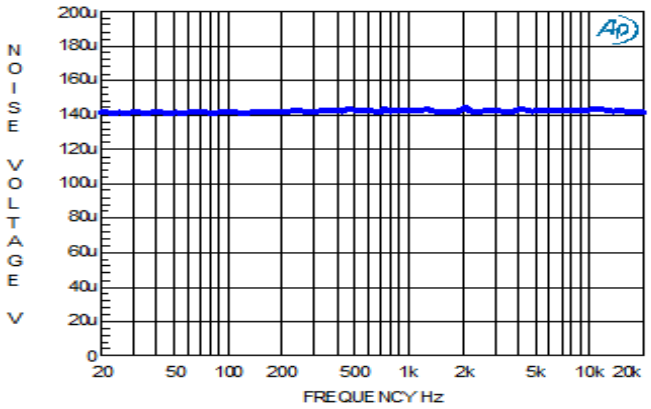


PSRR



V_{IN} = 3.3V, V_{OUT} = 1.6V, I_{OUT} = 100mA

Noise Level



V_{IN} = 3.3V, V_{OUT} = 1.6V, I_{OUT} = 100mA

Application Information

Capacitors Selection

Select carefully the external capacitors carefully to ensure stability and performance. Place the externally capacitors close to the IC with a distance no longer than 0.5 inches.

The input capacitor C_{IN} with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The LTS7001 is specifically designed to work with low ESR ceramic output capacitor in space-saving and performance consideration. A 1uF ceramic capacitor is adequate for stable operation. However, for best load and line transient response, output capacitor larger than 4.7uF is recommended.

Power Supply Rejection Ration (PSRR)

PSRR is a measure of how well a circuit rejects ripple coming from the input power supply at various frequencies and is very critical in many RF and wireless applications. PSRR is defined as the gain from the input ripple to output ripple over a wide frequency range (10Hz to 10MHz), Note that at heavy load measuring, ΔV_{IN} will cause temperature deviation. Temperature will cause ΔV_{OUT} voltage. So the heavy load PSRR measuring includes temperature effect.

Thermal Consideration

The maximum power dissipation is specified as:

$$P_{D(MAX)} = \frac{(125^{\circ}C - TA)}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance.

The LTS7001 features thermal protection that shuts down the IC if the junction temperature is higher than 160^{O}C. However, the power dissipation should be well designed to keep the continuous junction temperature below 125^{O}C for maximum reliability.

θ_{JA} depends on the thermal resistance of the package, PCB layout, surrounding airflow. For SOT-23-5 package, the thermal resistance θ_{JA} is 250^{O}C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at TA = 25^{O}C can be calculated as:

$$P_{D(MAX)} = \frac{(125^{O}C - 25^{O}C)}{250^{O}C/W} = 0.4W$$

For WDFN1.6x1.6-6L package, the thermal resistance θ_{JA} is 150^{O}C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at TA = 25^{O}C can be calculated as:

$$P_{D(MAX)} = \frac{(125^{O}C - 25^{O}C)}{150^{O}C/W} = 0.67W$$

Because of the small size of the TSOT23-5 package, it is very important to use a good thermal PC board layout to maximize the allowable power dissipation. The thermal path for the heat generated by the IC is from the die to the copper lead frame, through the package (especially the ground lead), to the PCB board cooper. The PC board copper. The PCB board copper is the heat sink. The footprint copper pads should be as wide as possible and expand out to larger copper areas to spread and dissipate the heat to the surrounding ambient. Feed through via to inner or backside copper layer are also useful in improving the overall thermal performance of the LDO regulator. Other heat sources on the board, not related to the LDO regulator, must also be considered when designing a PC board layout because they will affect overall temperature rise and the maximum allowable power dissipation. The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with the device mounted on topside.

Table 1. Measured Thermal Resistance (2-Layer Board)

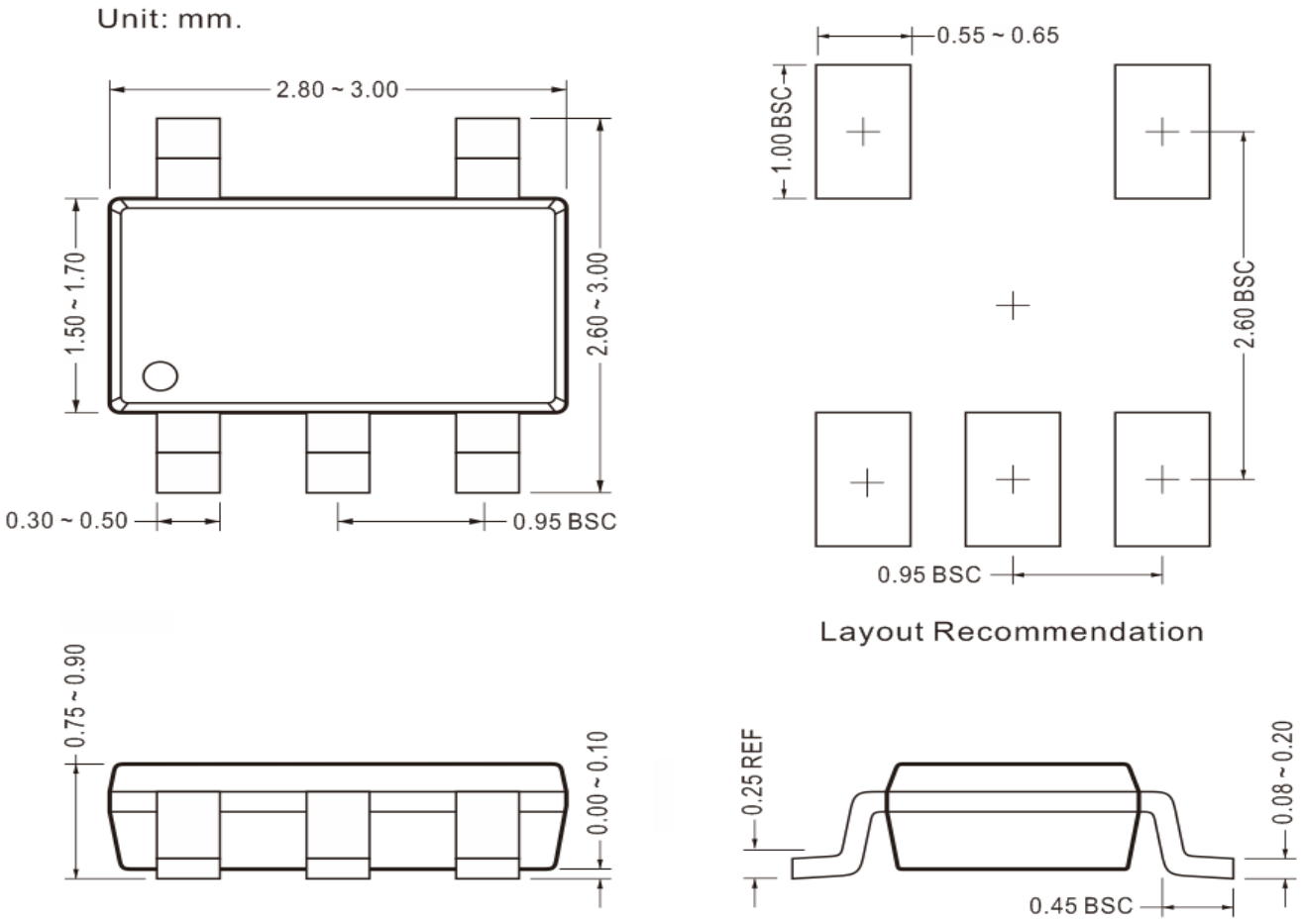
Copper Area(mm2)		Board Area (mm2)	θ_{JA} (^{O}C/W)
Top Side	Back Side		
2500	2500	2500, 2-Layer	125
1000	2500	2500, 2-Layer	125
225	2500	2500, 2-Layer	130
100	2500	2500, 2-Layer	135
50	2500	2500, 2-Layer	150

Layout Considerations

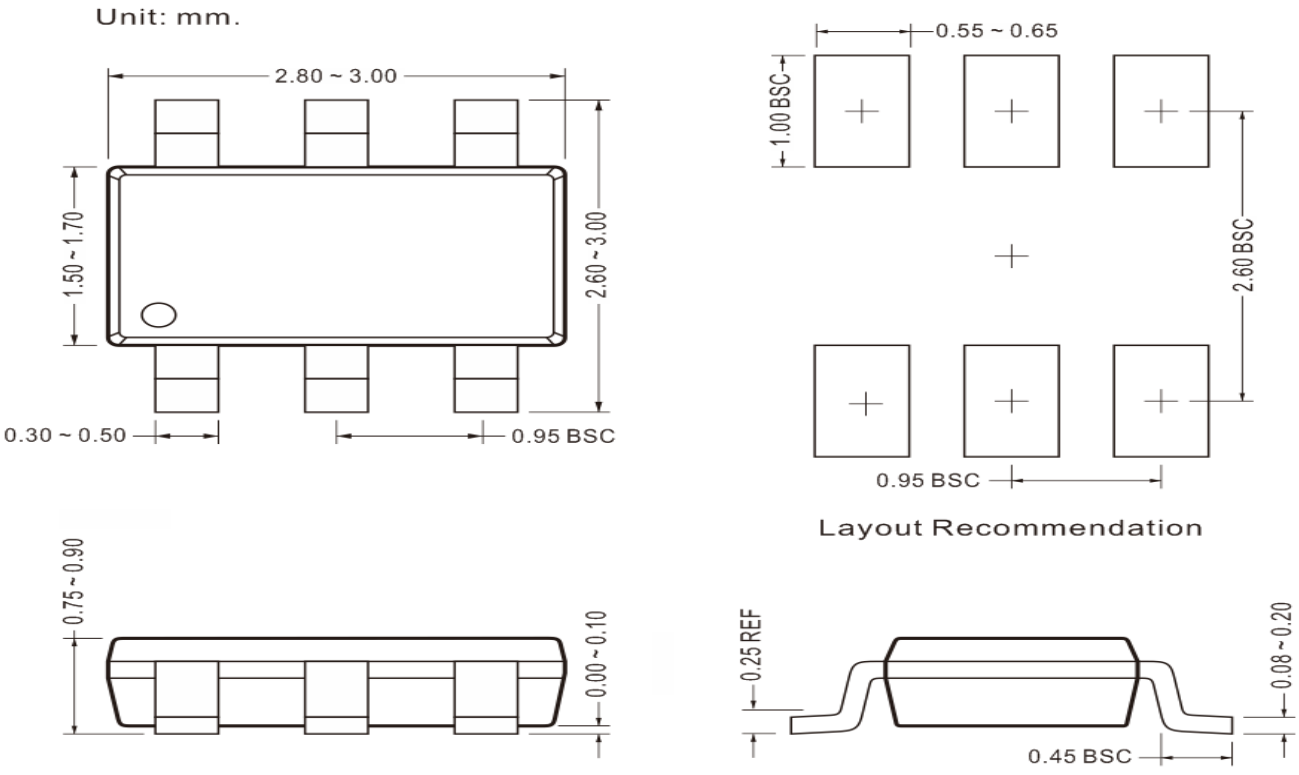
Careful PCB Layout is necessary for better performance. The following guidelines should be followed for good PCB layout.

- Place the input and output capacitors as close as possible to the IC.
- Keep V_{IN} and V_{OUT} trace as possible as short and wide.
- Use a large PCB ground plane for maximum thermal dissipation.

Package Information – TSOT23-5

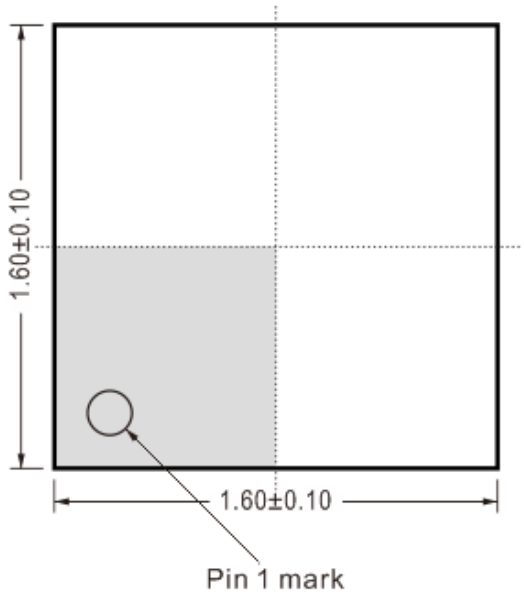


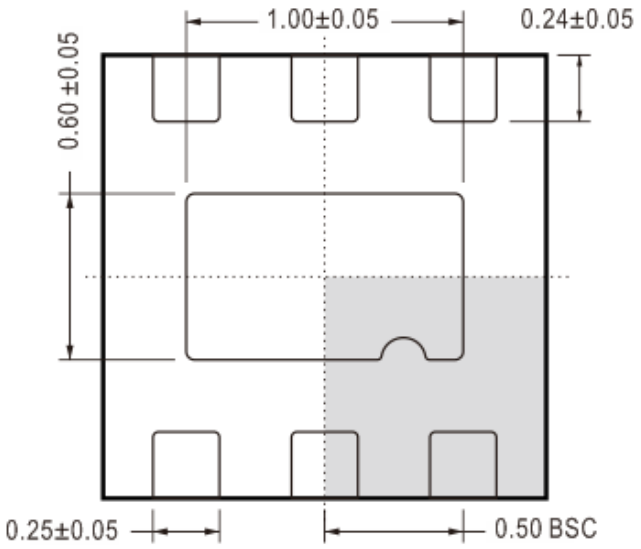
Package Information – TSOT23-6



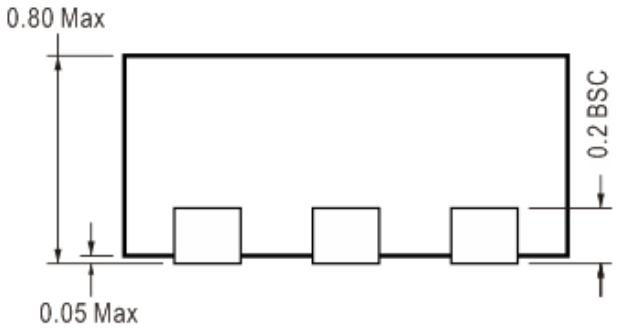
Package Information – WDFN1.6x1.6-6L

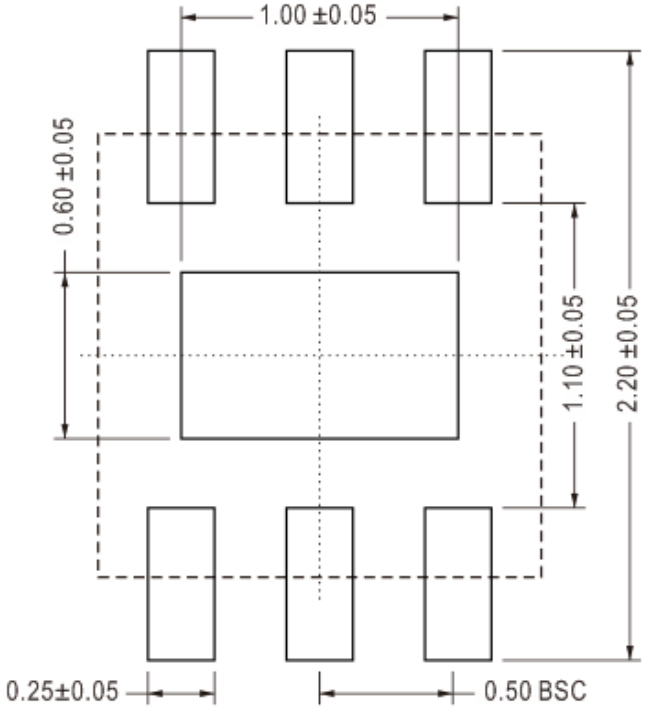
Unit: mm.





Bottom View - Exposed Pad





Recommended Solder Pad Pitch and Dimensions