USB-Friendly Li-Ion Battery Charger With Smart Power-Path Management

General Information

The LTS6002 is an integrated Li-ion linear charger with smart system power path management targeted at space-limited portable applications. The device operates from either a USB port or AC adapter and supports charge current up to 1A. DC Input current limit can be set up to 1.5A, while USB input current can be set to 0.1A, 0.5A or 0.9A. The LTS6002A battery to output power can be turned off by BAT_OFF pin to save battery power. The LTS6002B input power can be turned off by VIN_OFF pin, after that output power should support by Li-Ion battery.

The LTS6002 charges battery with a minimum current when the battery voltage is lower than 2.8V. The charger works with fixed current when the battery voltage is between 2.8V and 4.2V, and the charger works with fixed voltage when the battery voltage is 4.2V. The voltage level could be set by an I^2C interface.

The LTS6002 provides a programmable time-out function that initiates fault alarm if charge cycle is not complete within the time-out period. Other features include input over-voltage protection, thermal regulation charge current, NTC thermistor interface and automatic recharge.

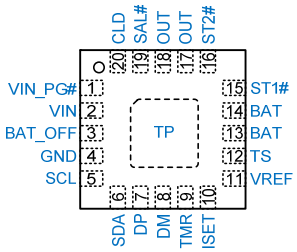
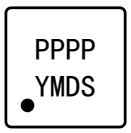
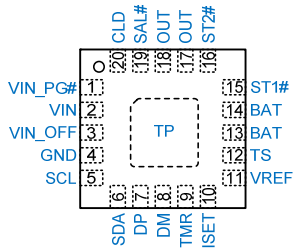
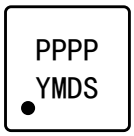
Wide input voltage range with input overvoltage protection supports unregulated adapters. Accurate USB input current limit and start up sequence allow the LTS6002 to meet USB-IF specification.

The LTS6002 features smart power path management (SPPM) that powers the system while simultaneously and independently charging the battery. The SPPM circuit reduces the charge current when the input current limit causes the system output to fall to the SPPM threshold; thus, supplying the system load at all times while monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. The LTS6002 is available in the WQFN3x3-20L packages.

Features

- Complete Linear Charger for Single Cell Lithium-Ion Battery
- I^2C Interface
- 0.9% Charge Voltage Accuracy
- Programmable Charge Current up to 1A
- Programmable Charge Current up to 4.35V
- Programmable Charge Termination Current
- C/10 Trickle Mode Charge
- Charge Status and Fault Indication
- NTC Interface for Battery Temperature Sensing
- Auto Input Source Detection (DP, DM Pins)
- Input Over-voltage Protection
- Input Current Limit
- RoHS Compliant and Halogen Free

Pin Configuration

Pin Configuration	Top Marking
	
	

PPPP: Product Code
YMDS: Date Code

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YMDS: Date Code

Applications

- Battery-Powered Devices
- Hand Held Devices

Typical Applications Circuit

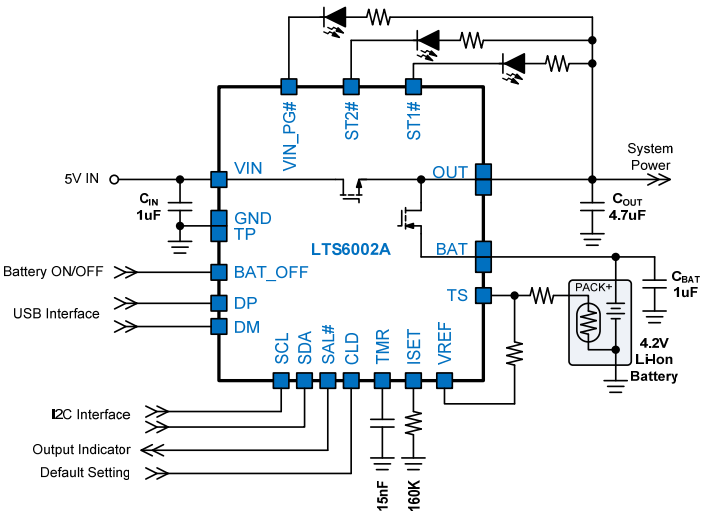


Figure 1-1. LTS6002A Application Circuit

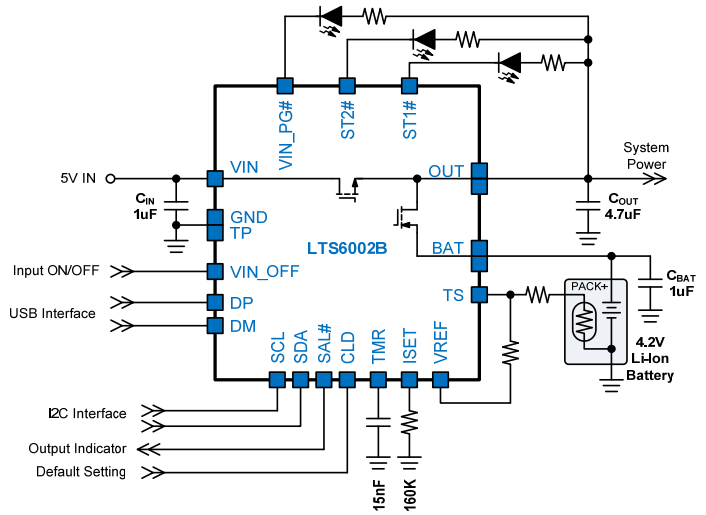


Figure 1-2. LTS6002B Application Circuit

Ordering Information

LTS6002 □□□□

Option:
A: BAT_OFF function
B: VIN_OFF function

Package Type:
Q3F:WQFN3x3-20L

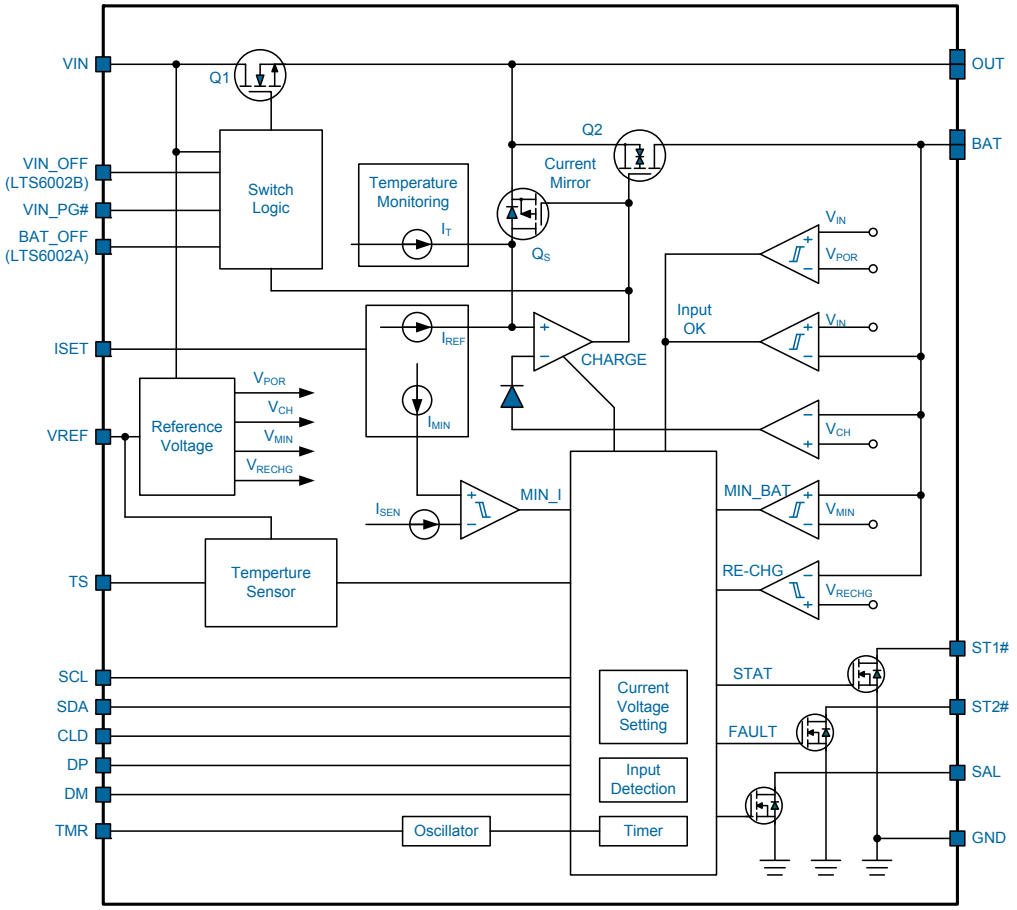
Ordering Number	Package	Top Marking (Product Code)	Note
LTS6002AQ3F	WQFN3x3-20L	A050	Support BAT Off Function
LTS6002BQ3F	WQFN3x3-20L	A051	Support VIN Off Function

Note 1. Leading TECH products are RoHs compliant and compatible with the current requirement of IPC/JDEC J-STDM020 and are suitable for use in SnPb or Pb-Free soldering processes.

Functional Pin Descriptions

Pin No.	Pin Name	Description
1	VIN_PG#	**Open-drain Input Indication Output**. VIN_PG# pulls to GND when a valid input source is detected. VIN_PG# is high-impedance when the input power is not within specified limits. Connect VIN_PG# to the desired logic voltage rail using a 1kΩ-100kΩ resistor, or use with an LED for visual indication.
2	VIN	**Input Power Connection**. Connect VIN to the external DC supply (AC adapter or USB port). The input operating range is 4.5V to 5.8V. The input can accept voltages up to 26V without damage but operation is suspended. Connect bypass capacitor 1uF to 10uF to GND.
3	BAT_OFF	**LTS6002A: BAT_ON/OFF.** Logic high turns on the BAT to OUT power. Internal pull-high 5MΩ to BAT.
	VIN_OFF	**LTS6002B: VIN ON/OFF Control.** Logic high turns off the input power. Internal pull-low 100kΩ to GND.
4	GND	**Ground**. Connect to the thermal pad and to the ground rail of the circuit.
5	SCL	**Clock Input for Serial Interface.** An external pull-up resistor is needed.
6	SDA	**Data Input/Output for Serial Interface.** An external pull-up resistor is needed.
7	DP	**USB Port D+ Input Connection.**
8	DM	**USB Port D- Input Connection.**
9	TMR	**Timer Programming Input**. TMR controls the pre-charge and fast-charge safety timers. Connect 15nF capacitor between TMR and GND to program the timers a desired length.
10	ISET	**Adjustable Charging Current Programming Input.** Connect a resistor from ISET to GND program the maximum charging current.
11	VREF	**Reference Output.** This pin outputs a 2.8V voltage source when the VIN is above POR threshold level and the charger is enabled. Connect bypass capacitor 1uF to GND
12	TS	**External NTC Thermistor Input**. Connect the TS input to the NTC thermistor in the battery pack.
13,14	BAT	**Charger Power Stage Output and Battery Voltage Sense Input**. Connect BAT to the positive terminal of the battery. Bypass BAT to GND with a 1uF ceramic capacitor.
15	ST1#	**Open-Drain Charging Status Indication Output**. ST1# pulls to low when the battery is charging. ST1# is high impedance when charging is complete or charger is disabled. Connect ST1# to the desired logic voltage rail using a 1kΩ-100kΩ resistor, or use with an LED for visual indication.
16	ST2#	**Open-Drain Charging Fault Indication**. This pin is an open-drain output indicating fault status. This pin is pulled to low under cell temperature fault, and time-out condition. Connect ST2# to the desired logic voltage rail using a 1kΩ-100kΩ resistor, or use with an LED for visual indication.
17,18	OUT	**System Supply Output**. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to VBAT except when VIN_OFF is high. Connect OUT to the system load. Bypass OUT to GND with a 4.7uF to 10uF ceramic capacitor.
19	SAL#	**Output for Serial Interface.** An external pull-up resistor is needed.
20	CLD	**Current Limit Default.** Logic low sets default current limit to be 0.1A. Logic high sets default current limit to be 0.5A. 100kΩ internal pull-low resistor is connected.
Thermal Pad	TP	**Thermal Pad.** Must tie this pad to the ground island/plane through the lowest impedance connection available. This pin is also used as heat-sink of the IC and should be well-soldered to the PCB for optimal thermal performance.

Functional Block Diagram



Operation Principles

Chip Enable

The LTS6002 device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. It also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port.

The device features smart power path management (SPPM), which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. When charging from a USB port, the input power path management circuit reduces the input current if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

Under Voltage Lockout (UVLO)

The LTS6002 remains in power down mode when the input voltage at the VIN pin is below the under-voltage threshold (UVLO).

For the LTS6002A, during the power down mode the host commands at the control input (BAT_OFF) are logic low level. The Q2 FET disconnected between BAT and OUT pins is off and the quiescent current small than 10uA.

For the LTS6002B, during the input power disconnect mode the host commands at the control inputs (VIN_OFF) are logic low level. The Q1 FET connected between VIN and OUT pins is off, and the status outputs ST1# and VIN_PG# are high impedance. The Q2 FET that connects BAT to OUT is ON.

Auto Input Source Detection (DP, DM pins)

The LTS6002 features Auto Input Source Detection to identify adapter or USB port power source is connected. The input current limit default setting is selected by CLD

pin (L=0.1A, H=0.5A). After an adaptor source is detected, the LTS6002 will transfer from the default input current limit level to the 1.5A. If a USB port is detected, the input current limit will stay at the default limit level. If a different input current limit level is desired, WRITE I²C bit7 and bit6 in index3 to switch other USB mode current limit setting. The DP and DM pin connected in the LTS6002 are disconnected within 100ms after the DP or DM lines being pulled high (start of detection) to minimize any interaction between the charger detection pins and the USB normal communications.

Power On

When V_{IN} exceeds the UVLO threshold, the LTS6002 powers up. While VIN is below V_{BAT} + $V_{IN(DT)}$, the host commands at the control inputs (VIN_OFF) are ignored. The Q1 FET connected between VIN and OUT pins is off, and the status outputs ST1# and VIN_PG# are high impedance. The Q2 FET that connects BAT to OUT is ON. (If VIN_OFF is high, Q1 is off). During this mode, the V_{OUT} circuitry is active and monitors for overload conditions on OUT.

Once V_{IN} rises above V_{BAT} + $V_{IN(DT)}$, VIN_PG# is driven low to indicate the valid power status and the VIN_OFF inputs are ready. The device enters standby mode or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. (If VIN_OFF is high, FET Q1 is off). During this mode, the V_{OUT} circuitry is active and monitors for overload conditions on OUT.

When the input voltage at VIN is within the valid range: V_{IN} > UVLO AND V_{IN} > V_{BAT} + $V_{IN(DT)}$ AND V_{IN} < V_{OVP}, indicate that the USB suspend mode is not enabled all internal timers and other circuit blocks are activated.

If no short conditions exists, the device switches on the input FET Q1 with a 100mA current limit to checks for a short circuit at OUT. When VOUT is above V_{SC}, the FET Q1 switches to the current limit threshold set by I²C interface and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is regulating), and the device continuously monitors the status of VIN_OFF as well as the input voltage conditions.

Table 1. VIN_OFF Control

VIN_OFF Pin	Bit1 in Index3	Status
>1.5V	0	WRITE OK.
	1	But IC not yet action
<0.4V	0	VIN ON
	1	VIN OFF

Input Over Voltage Protection

The LTS6002 accepts inputs up to 26V without damage. Additionally, an overvoltage protection (OVP) circuit is implemented that shuts off the internal LDO and discontinues charging when V_{IN} > V_{OVP}. When in OVP, the system output (OUT) is connected to the battery and VIN_PG# is high impedance. Once the OVP condition is removed, a new power on sequence starts (See the *Power On* section). The safety timers are reset and a new charge cycle will be indicated by the ST1# output.

Power Path Management

The LTS6002 features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to VIN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

Smart Power Path Selector

As shown in Figure 2, the LTS6002 features a Smart Power Selector to make the best use of limited input power. The function operation is as following statement:

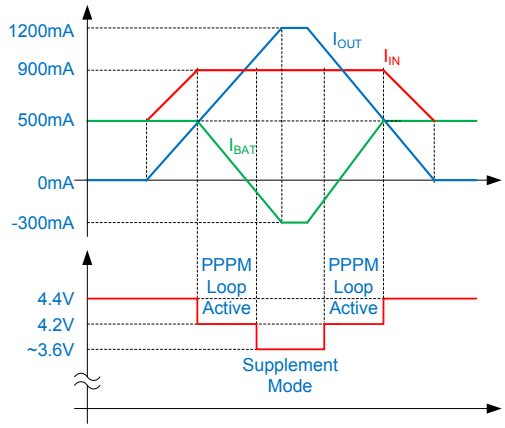


Figure 2. PPM and Supplement Mode.

- Priority Power Path Management Mode

In case of the summation of charging and OUT current exceeds USB mode (USB100, USB500 and USB900) or adaptor input current limit, it causes a decrease in OUT voltage. PPPM mode is trigged when the fallen OUT voltage meet V_{PPPM}. In PPPM mode, for the sake of maintaining OUT voltage, the charging current is reduced to provide more load current request.

- Supplement Mode

As above mentioned, while the LTS6002 enters the PPPM mode, the battery is charged with residual power from the input. When load current continues to rise to input current limit, the charging current will fall to zero. When the load current request is more than input current limit, there will be another decrease in output voltage. Once the fallen output voltage meet V_{BSUP1}, the BAT-OUT FET works as a switch and the battery supplies power to system load.

Input Source Connected (Adapter or USB)

With a source connected, the smart power-path management (SPPM) circuitry of the LTS6002 monitors the input current continuously. The output for the LTS6002 is regulated to a fixed voltage ($V_{O(REG)}$). This allows for proper startup of the system load even with a discharged battery. The current into VIN is shared between charging the battery and powering the system load at OUT. The LTS6002 has internal selectable current limits of 100mA (USB100) and 500mA (USB500) for charging from USB ports.

The LTS6002 is USB IF compliant for the inrush current testing. The USB spec allows up to 10uF to be hard started, which establishes 50uC as the maximum inrush charge value when exceeding 100mA. The input current limit for the LTS6002 prevents the input current from exceeding this limit, even with system capacitances greater than 10uF. Note that the input capacitance to the device must be selected small enough to prevent a violation (<10uF), as this current is not limited. Figure 2 demonstrates the startup of the LTS6002 and compares it to the USB-IF specification.

OUT Power

An LDO regulates OUT voltage at 4.4V for system power. The LDO features internal soft start that minimizes the inrush current from supply inputs. The output voltage ramp-up time is about 2ms. If no valid input source is recognized, the BAT-OUT FET is on to supply OUT current.

Battery Charging

For the LTS6002 CHG_EN default High to initiate battery charging. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

The LTS6002 charges battery with a minimum current when the battery voltage is lower than 2.8V. The charger works with fixed charge current when the battery voltage is between 2.8V and 4.2V, the charge current is programmable by an external resistor. The charger works with fixed charge voltage when the battery voltage exceeds programmed VBAT charge voltage.

Charge Cycle

A charge cycle can be initiated by anyone of the following events:

- CHG_EN = 1 (bit2 in index3).
- A new battery is inserted (detected by TS pin).
- The battery voltage drops below a recharge threshold after completing a charge cycle.
- Recovery from a battery over temperature or under temperature fault.
- Recovery from VIN OFF. For LTS6002B only

A charge cycle consists of three charge modes: trickle mode (TKM), constant current mode (CCM), and constant voltage mode (CVM) as shown in Figure 3.

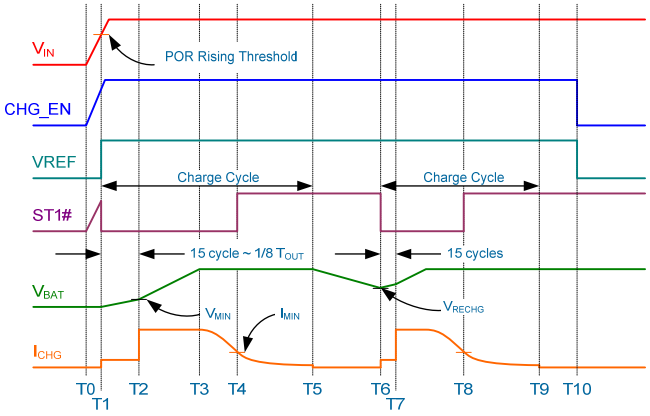


Figure 3. Li-Ion Charge Cycle.

In the pre-charge phase, the battery is charged at with the pre-charge current (I_{PRECHG}). Once the battery voltage crosses the V_{MIN} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{MIN}, the ST1# pin indicates charging done by going high-impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the PPM loop or the $V_{IN(LOW)}$ loop.

Disable the Charge loop

The charge loop is disabled under any one of the following condition:

1. under voltage lockout (UVLO) or over voltage protection (OVP)
2. CHG_EN (bit2 in index3)is set to 0
3. Time-out fault and cell temperature fault.
4. VIN OFF by pulling high VIN_OFF pin, this for LTS6002B only
5. VIN OFF by I^2C interface (bit1 = 1 in index3) , this for LTS6002B only

The input voltage at VIN pin is continuously monitored for UVLO and OVP. The LTS6002 releases UVLO and

resets the I²C registers regarding the charger when the VIN enters the operation window. Furthermore, the LTS6002 releases OVP and keep the I²C registers.

Charge Current Translator

The LTS6002 current limit is adjustable up to 1.5A. The valid resistor range is 66.5kΩ (1.2A charge current) to 160KΩ (500mA charge current).

When the charger is enabled, internal circuits generate a current proportional to the charge current at the ISET input. The current out of ISET is regulated to 0.8V reference voltage when they are left open. External resistors RISET is connecting between ISET to ground programs reference current ISET.

$$I_{CHGREF}(mA) = \frac{0.8(V)}{R_{ISET}(k\Omega)} \times 10^5$$

The reference current ICHGREF is a programmed from 1/8 to 1 time by I²C interface (index2, bit4, bit3 and bit2), The charge current ICHG at fast charging will be 100,000 times of ISET; for example, if 160k RISET is taken, then bit4,bit3 and bit2 in index2 is written to 1, the ICHG at fast charging will be calculated as :

$$I_{CHGREF} = \frac{0.8}{160} \times 10^5 = 500\,(mA)$$

Battery Turn-off (BAT_OFF Input)

The LTS6002A features a BAT_OFF input that allows the user to turn the FET Q2 off and disconnect the battery from the OUT pin. This is useful for disconnecting the system load from the battery, factory programming where the battery is not installed or for host side impedance track fuel gauging. BAT_OFF is internally pulled to BAT through ~5MΩ resistor.

Table 2. BAT_OFF Control

BAT_OFF Pin	VIN	Status
>1.4V	5V	Charger works
	Removal	VOUT=VBAT
<0.4V	5V	Charger works
	Removal	VOUT no power

Dynamic Charge Timers (TMR Input)

The LTS6002 contains internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a capacitor from TMR to GND. The oscillation period is described calculated using the following equation:

$$T_{OSC} = 2 \times 10^5 \times C_{TMR}\,(sec)$$

A 20-stage binary counter counts the timing oscillation to get a time base TBASE. It can be calculated as:

$$T_{BASE} = 2^{20} \times T_{OSC} = 2^{21} \times 10^5 \times C_{TMR}\,(sec)$$

For example, a 15nF CTMR results in a 3ms oscillation period and 0.8738 hours' time base. The total charge time TOUT is programmable from 2x to 8x of TBASE by I²C interface. If a charge cycle is not completed after TOUT expires, the LTS6002 shuts down the charger. The TKM also has a time limit TTKM calculated as follow:

$$T_{TKM} = \frac{1}{4} \times T_{BASE} = 2^{19} \times 10^5 \times C_{TMR}\,(sec)$$

The LTS6002 shuts down the charger, if the battery voltage does not reach 2.8V after TTKM expires.

Status Indicators (VIN_PG#, SAL#, ST1#, ST2#)

The LTS6002 contains open-drain outputs that signal its status. The VIN_PG# output signals when a valid input source is connected. VIN_PG# is low when (V_{BAT} + $V_{IN(PG)}$) < V_{IN} < V_{OVP}. When the input voltage is outside of this range, VIN_PG# is high impedance.

The LTS6002 has three indications: the SAL#, the ST1#, and the ST2# indication. (The status of ST1# and ST2# indication as shown in Table 2 and 3)

SAL#

The SAL# pin is used to indicate the data changed in the I²C SAL register. The alert pin is an open-drain logic output that is pulled low with the following conditions:

1. NTC protection condition: If the VTS for monitoring the battery pack is over higher or lower than threshold, charge cycle will suspend. Charge cycle will be enabled after VTS is recovery to normal threshold.
2. Charger time-out conditions: If time-out expires in charging, the charge cycle will suspend. Re-enable charging (bit2 in index3) can reset the timer.
3. TMR pin abnormal condition: If there is a short or open condition at TMR pin, charger is disabled.
4. Input OVP condition: If the VIN is over V_{OVP}, LTS6002 will be shut down. The LTS6002 will act after input voltage decreases to normal threshold again.
5. ISET pin abnormal condition: If there is a short or open condition at ISET pin, SAL# pin will be low and charger is disabled.

The pulled low SAL# is released at writing the bit0 of index3. If SAL is released without removing above

conditions then alert won't act again.

ST1# Indication

The ST1# pin is an open-drain logic output that is pulled low when the charger is in charge states. The pin will be Hi-Z at following conditions:

1) No battery connected or CHG_EN set to L

2) Fault condition by timer or NTC.

3) Charge done (EOC trigged).

The EOC condition is: the battery voltage is within the charge high voltage V_{CHG} and V_{RECHG} and the charge current falls below a user programmable EOC current threshold.

ST2# Indication

The ST2# pin is an open-drain logic output. The fault conditions include the battery NTC fault and the timer fault. The ST2# pin is an open-drain logic output that is pulled low when NTC fault occur. The ST2# pin flash once the timer fault is detected. The flash frequency, f = 1Hz

Table 3. VIN_PG# Status Indicator

Input State	VIN_PG# Output
$V_{IN} < V_{UVLO}$	Hi-Z
$V_{UVLO} < V_{IN} < V_{IN(PG)}$	Hi-Z
$V_{IN(PG)} < V_{IN} < V_{OVP}$	Low
$V_{IN} > V_{OVP}$	Hi-Z

Table 4. Charger Status Indicator

ST1#	ST2#	STATUS
L	Hi-Z	Charging
		Re-Charging
Hi-Z	Hi-Z	CHG_EN=L or No Battery (no BAT, NTC=H)
		Charge Done
Hi-Z	Flash	Charging Fault by Timer
Hi	L	Charging Suspend by NTC

Thermal Regulation and Thermal Shutdown

The LTS6002 contains a thermal regulation loop that monitors the die temperature. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous over temperature conditions result in a hiccup mode. During thermal regulation, the safety timers are slowed down proportionately to the reduction in current limit.

Note that this feature monitors the die temperature of the LTS6002. This is not synonymous with ambient temperature. Self-heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO associated with OUT. A modified charge cycle with the thermal loop active is shown in Figure 4. Battery termination is disabled during thermal regulation.

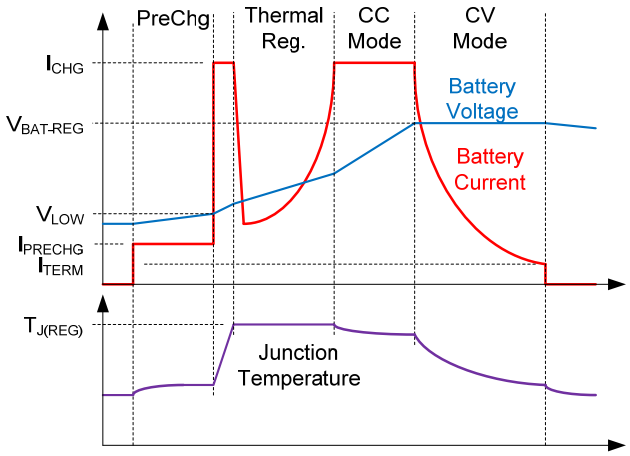


Figure 4. Charge Cycle Modified by Thermal Loop

Battery Pack Temperature Monitoring

The LTS6002 features an external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. Use a NTC thermistor to form a voltage divider at TS pin for monitoring the battery pack as shown in Figure 5. The LTS6002 stops charging if the voltage at TS pin is out of the window. The LTS6002 starts another charge cycle when the voltage at TS pin is within the window again.

The lower temperature boundary is V_{TMIN} = 2.1V that is 0.75 of the VREF bias voltage. where R_U is the pull-high resistor, R_L is the pull-low resistor, and $R_{NTC,L}$ is the thermistor resistance at low temperature limit. In case of the voltage at TS pin is higher than 2.52V (90% of VREF) indicates the battery is removed.

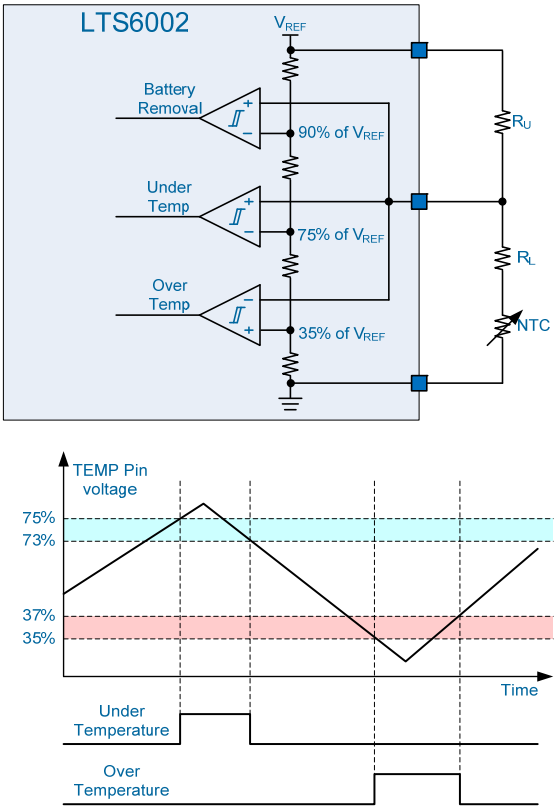


Figure 5 Battery Temperature Monitoring

I²C Function Description

The LTS6002 features I²C interface for charging charge current, charge voltage, and timer...etc..

I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as a change in data during this time is interpreted as a control signal.

I²C Start and Stop Conditions

Both SDA and SCL remain high when the bus is not busy. A high-to-low transition of SDA is defined as the start (S) condition while the SCL is high. A low-to-high transition of the SDA is defined as the stop (P) while SCL is high.

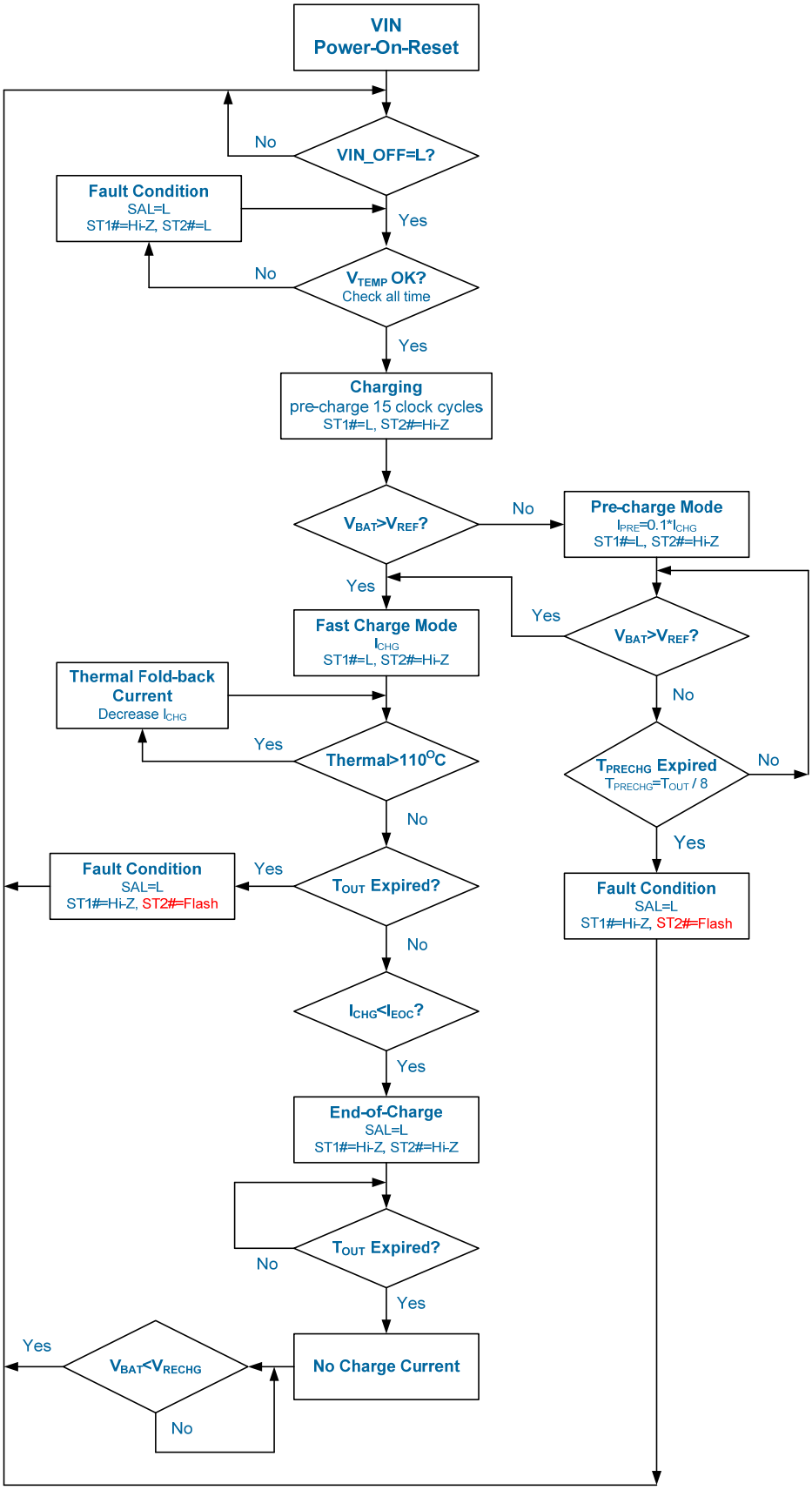
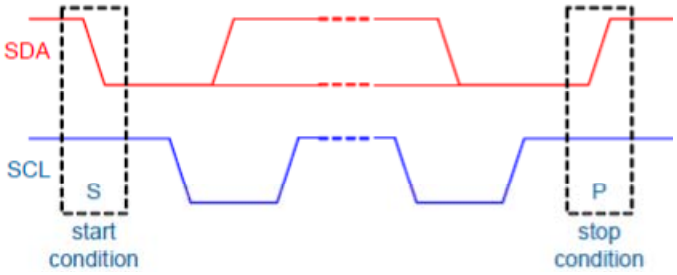
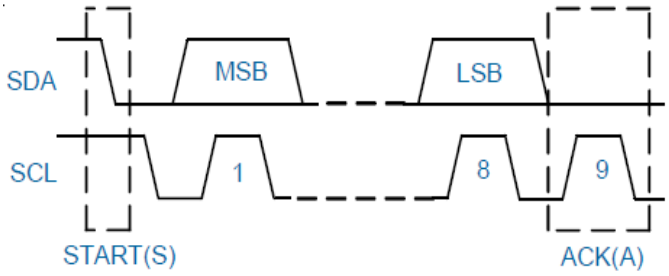


Figure 6. Battery Charging Flow





I²C Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (A). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address pulls SDA low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

I²C Version Code

The Chip ID code of the LTS6002 is 62H.

I²C Address

The Address of the LTS6002 for WRITE is 80H.

The Address of the LTS6002 for READ is 81H.

Read and Write Protocol

Write to a Single Register

S	Slave_addr+W [A7:A0]	AS	Reg_addr(index) [I7:I0]	AS	Reg_data [D7:D0]	AS	S

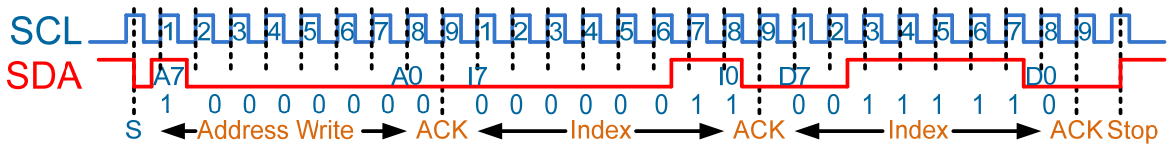


Figure 7. WRITE example, Write index 3 register

Read from a Single Register

S	Slave_addr+W [A7:A0]	AS	Reg_addr(index) [I7:I0]	AS	RS	Slave_addr+R [A7:A0]	AS	Reg_data [D7:D0]	AS	P

S=Start, P=Stop, AS=ACK from slave, NA=No ACK, RS=Pepeat Start

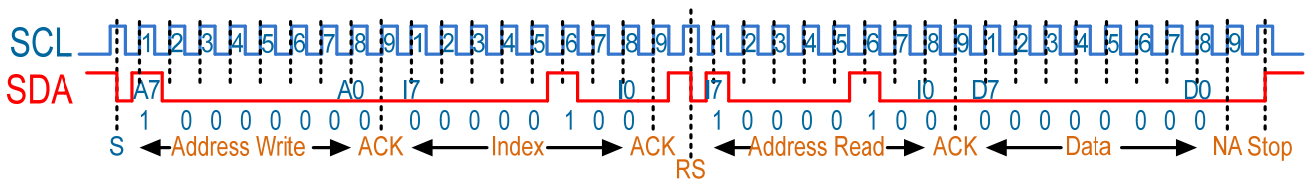


Figure 8. READ example, Read the index 4

I²C Command

Table 5. I²C Command Summary

Register Address		Data							
Index	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Index1	R	Chip ID Code: 62h							
Index2	R/W	Battery Voltage Setting			Charge Current Setting			EOC Current Setting	
Index3	R/W	VIN Current Limit		Total Charge Time Setting			CHG_EN	VIN_OFF	SAL Reset
Index4	R	Charger Time-out	TMR Open/Short	High Temp.	Low Temp.	VIN OVP	ISET Open/Short	Battery Removal	Reserve

Table 6. Index 2 data setting

Register Address		Data							
Index2	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Battery Voltage Setting			Charge Current Setting			EOC Current Setting	
R/W	83h	1	0	0	0	0	0	1	1
Bit	**Data**								
Bit7	Battery Voltage Setting	000: 4.00V 001: 4.05V 010: 4.10V 011: 4.15V **100: 4.20V** 101: 4.25V 110: 4.30V 111: 4.35V							
Bit 6									
Bit 5									
Bit 4	Charge Current Setting	**000: I_{CHGREF} *1/8** 001: I_{CHGREF} *2/8 010: I_{CHGREF} *3/8 011: I_{CHGREF} *4/8 100: I_{CHGREF} *5/8 101: I_{CHGREF} *6/8 110: I_{CHGREF} *7/8 111: I_{CHGREF} *8/8							
Bit 3									
Bit 2									
Bit 1	EOC Current Setting	00: I_{CHGREF} *1/5 01: I_{CHGREF} *1/10 10: I_{CHGREF} *1/15 **11: I_{CHGREF} *1/20**							
Bit 0									

Table 7. Index 3 data setting

Register Address		Data							
Index3	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		VIN Current Limit		Total Charge Time Setting			CHG_EN	VIN_OFF	SAL Reset
R/W	14h	0	0	0	1	0	1	0	0

Bit	Data
Bit 7	**00: 0.1A** 01: 0.5A 10: 0.9A 11: 1.5A
Bit 6	
Bit 5	000: T_{BASE} *2 001: T_{BASE} *3 **010: T_{BASE} *4** 011: T_{BASE} *5 100: T_{BASE} *6 101: T_{BASE} *7 110: T_{BASE} *8 111: No time-out
Bit 4	
Bit 3	
Bit 2	0: Disable charger **1: Enable charger**
Bit 1	**0: VIN on** 1: VIN off
Bit 0	0: Charger in normal operation 1: Write “1” to reset alarm

Table 8. Index 4 data setting

Register Address		Data							
Index4	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Charger Time-out	TMR Open/Short	High Temp.	Low Temp.	VIN OVP	ISET Open/Short	Battery Removal	Reserve
R	00h	0	0	0	0	0	0	0	0

Bit	Data
Bit 7	0: Normal 1: Time-out
Bit 6	0: Normal 1: Open/Short
Bit 5	0: Normal 1: High temperature
Bit 4	0: Normal 1: Low temperature
Bit 3	0: Normal 1: VIN OVP
Bit 2	0: Normal 1: Open/Short
Bit 1	0: Normal 1: Battery removal
Bit 0	x

Absolute Maximum Ratings (Note 1)

Input Supply Voltage (V_{IN}) ..... -0.3V to 26V
Other Pins ..... -0.3V to 6.0V
BAT Pin ..... -0.3V to 5.5V
Charge current.....1.5A
ESD (Note 2)
- Human Body Mode 2kV
- Machine Mode 200V

Thermal Information

Continuous Junction Temperature Range ..... -40°C to 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 second) ..... 260°C
Package Thermal Resistance (Note 3)
- WQFN3x3-20L, θ_{JA} ..... 68°C/W
- WQFN3x3-20L, θ_{JC} ..... 7°C/W

Maximum Power Dissipation, P_D @ T_A = 25°C (Note 4)
- WQFN3x3-20L 1.47W

Recommended Operation Conditions

Continuous Junction Temperature Range ..... -40°C to 120°C
Ambient Temperature Range ..... -40°C to 85°C
Input Voltage Range (V_{IN}) ..... 4.5V to 5.5V

Note 1: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

Note 2: This device is sensitive to electrostatic discharge. Follow proper handling procedures.

Note 3: The Thermal Resistance specifications are based on a JEDEC standard JESD51-3 single-layer PCB. θ_{JA} will vary with board size and copper area.

Note 4: The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J-MAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{D(MAX)} - T_A)/\theta_{JA}$. The maximum power dissipation is determined using T_A = 25°C, and $T_{J(MAX)}$ = 125°C.

Electrical Characteristics

V_{IN} = 5V, V_{BAT} = 3.6V, and T_A = 25°C unless otherwise specified.

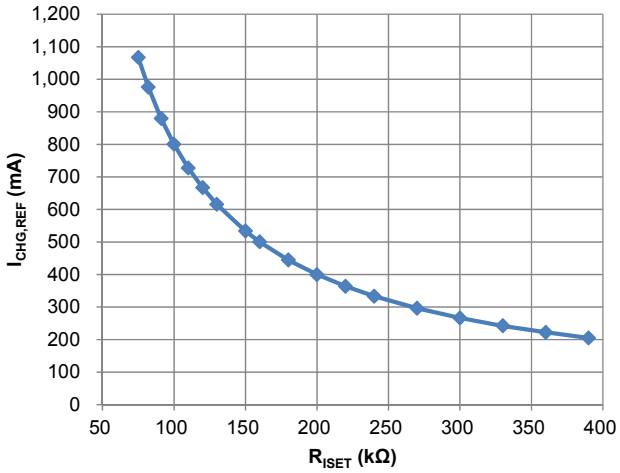
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Supply Voltage, VIN						
Input POR rising Threshold			--	3.5	--	V
Input POR Hysteresis		VIN falling	--	0.2	--	V
Input Power Detection Threshold	$V_{IN(DT)}$	Input power detected when $V_{IN} > V_{BAT} + V_{IN(DT)}$, V_{BAT}=3.6V, V_{IN}=3.5V→4V	30	80	130	mV
Hysteresis on $V_{IN(DT)}$	V_{hys}	V_{BAT}=3.6V, V_{IN}=4V→3.5V	20	--	50	mV
Input Power Detection Deglitch Time	t_{PGG}	VIN=0V→5V or VIN=7V→6V VIN_PG# = Hi-Z→L	--	1.2	--	ms
	t_{PGN}	VIN=5V→3V or VIN=6V→7V VIN_PG# = L→Hi-Z	--	20	--	ms
Input OVP	V_{OVP}	VIN rising	5.6	5.8	6.0	V
Input OVP Hysteresis		VIN falling	--	0.2	--	V
Input Voltage DPM Threshold	V_{IN-DPM}	USB500 & USB100 mode.	4.35	4.5	4.63	V
Input Supply Current			--	1	2	mA
VIN to OUT Resistance		V_{IN}=4.3V, I_{IN}=1A, V_{BAT}=4.2V	--	200	350	mV
VIN Current Limit	$I_{IN,LIM}$	1.5A mode	1.35	1.5	1.65	A
		USB900 mode	810	855	900	mA
		USB500 mode	450	475	500	mA
		USB100 mode	80	90	100	mA
OUT						
Output Voltage	$V_{O(REG)}$		4.35	4.40	4.45	V
Output Voltage SPPM Threshold	V_{DPPM}		--	4.2	--	V
OUT to BAT Resistance		V_{BAT}=3.7V, I_{OUT} =1A	--	50	90	mV
Output Short-Circuit Detection Threshold	$V_{O(SC)}$	V_{BAT} -V_{OUT} @ battery supplement mode	200	250	300	mV
	$V_{O(SC,IN)}$	V_{IN}=5V, I_{IN} reduce to 0.1A	--	1.5	--	V
Output Short-Circuit Deglitch Time	t_{SC}		--	12	--	Us
Output Short-Circuit Blanking Time	t_{SCB}		--	1	--	Ms
Output Short-Circuit Recovery Time	t_{SC_R}		--	60	--	Ms
Charger Output						
Output Voltage	$V_{BAT(REG)}$		4.16	4.20	4.23	V
Trickle Charge Threshold Voltage	V_{TRK}		2.74	2.80	2.86	V
Recharge Voltage Threshold	V_{RC}		--	V_{BAT}-200mv	--	V
BAT pin input current @ power down	$I_{BAT(down)}$	BAT_OFF=floating V_{BAT}=4.2V, V_{IN}=GND ,V_O=no load	--	1	3	uA
		BAT_OFF=0V (LTS6002A) V_{BAT}=4.2V, V_{IN}=GND ,V_O=no load	--	2	5	uA
Charge Current						
Constant Charge Current	I_{CHG}	I_{SET}=100kΩ, V_{BAT}=3.7V, index2=93h	450	500	550	mA

Trickle Current Accuracy	I_{TRK}	I_{SET}=100kΩ, V_{BAT}=2.5V, 0.1*I_{CHG} index2=93h	40	50	60	mA
End-of-Charge Current Accuracy	I_{EOC}	End-of-charge Current=100mA, V_{BAT}=4.2V, I_{SET}=160kΩ, index2=80h	90	100	110	mA
VREF						
V_{REF} Output Voltage			2.74	2.80	2.86	V
V_{REF} Sourcing Current		Decrease to 98% of VREF	2	--	--	mA
V_{REF} Leakage Current		V_{REF}=3.3V, CHG_EN=L	--	--	1	uA
Oscillator						
Oscillation Period		C_{TMR}=15nF	2.7	3.0	3.3	ms
Logic Input and Output						
VIN_OFF, BAT_OFF Input High			1.4	--	5.5	V
VIN_OFF, BAT_OFF Input Low			0	--	0.4	V
Leakage Current @ VIN_PG#, SAL#, ST1#, ST2#		V_{IN}=0V	--	--	1	uA
Sink Current @ VIN_PG#, SAL#, ST1#, ST2#		I_{SINK}=5mA	--	--	0.25	V
DP/DM DETECTION						
Detection Time from start of DP/DM detection to latched output		t=0 at DM pulled -up > 0.5V or DP pulled up externally, >0.8V	--	--	150	ms
Bias at DP, during detection routine		Can source at least 200uA	0.475	0.6	0.7	V
Current sink at DM pin, during detection routine		V_{DM}=0.5V	50	100	150	uA
DP leakage when not in detection mode		V_{DP}=5V	--	--	1	uA
DM leakage when not in detection mode		V_{DM}=5V	--	--	1	uA
DM Comparator Threshold Rising			0.25	--	0.35	V
DM Comparator Hysteresis			--	42	--	mV
DP Comparator Threshold Rising			0.75	--	0.875	V
DP Comparator Hysteresis			--	42	--	mV
Temperature Monitoring						
Low Temperature Threshold			--	75	--	%VREF
High Temperature Threshold			--	35	--	%VREF
Temperature Hysteresis			--	2	--	%VREF
TS pin Leakage Current		TS=3.3V	--	--	1	uA
Charge Current Foldback Threshold			95	110	125	^{0}C
Over Temperature Protection			--	150	--	^{0}C
Over Temperature Hysteresis			--	15	--	^{0}C
I^2C Interface						
Clock Frequency			10	--	400	kHz
Bus-Free Time Between START and STOP			1.3	--	--	us
Hold Time Repeated START Condition			0.6	--	--	us
SCL Low Period			1.3	--	--	us

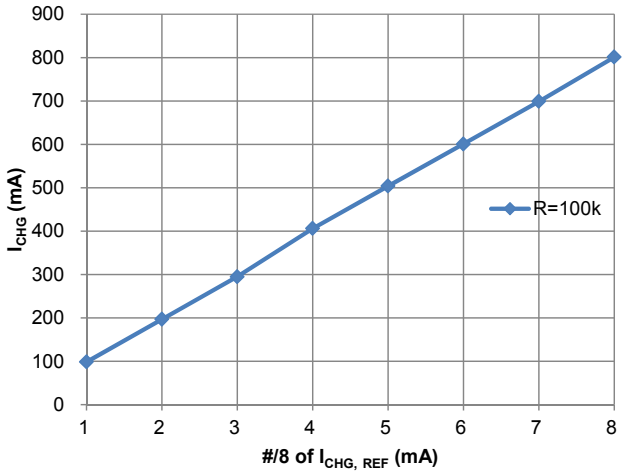
SCL High Period			0.6	--	--	us
Set-Up Time Repeated START Condition			0.6	--	--	us
SDA Hold Time			100	--	--	ns
SDA Set-Up Time			100	--	--	ns
Maximum Pulse Width of Spikdes that Must be Suppressed by the Input Filter of Both SDA and SCL Signals			--	50	--	ns
Set-Up Time for STOP Conditions			0.6	--	--	us

Typical Characteristics

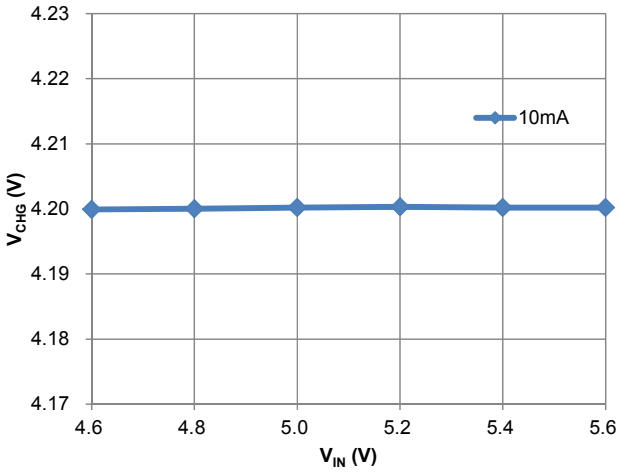
Charge Current vs ISET Resistor



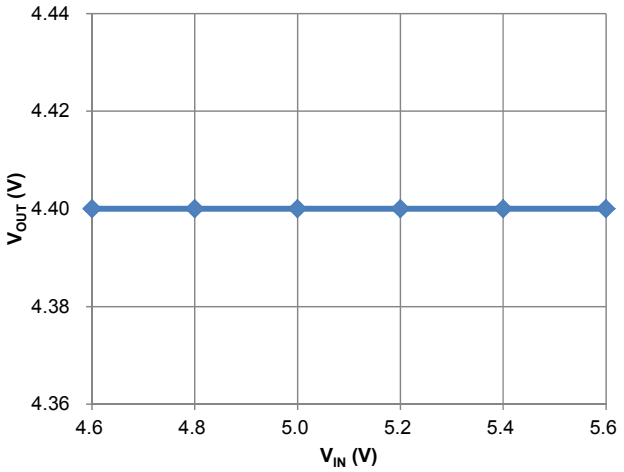
Charge Current vs I²C Setup Step



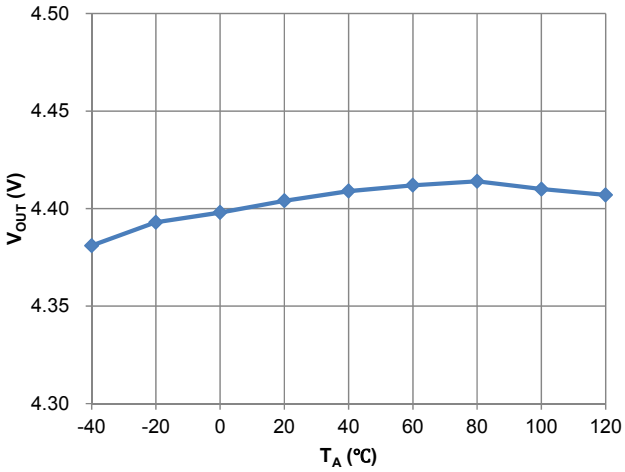
Charge Voltage vs Input Voltage



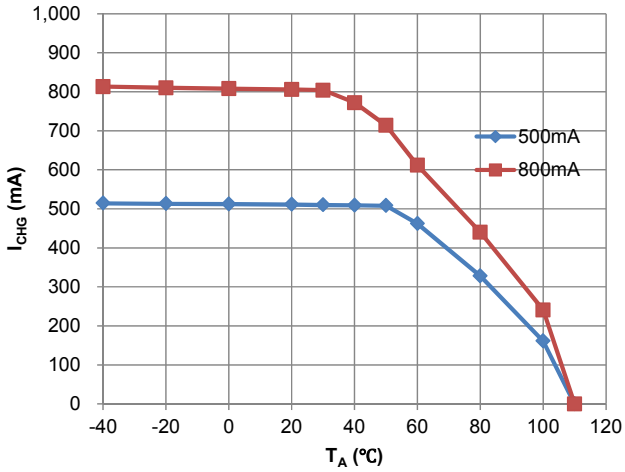
OUT Voltage vs Input Voltage



OUT Voltage vs Temperature

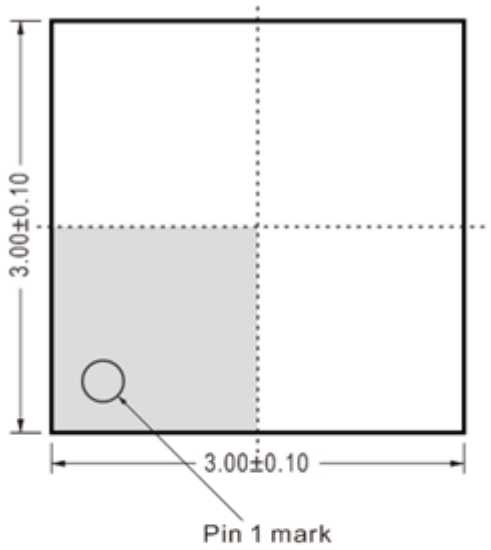


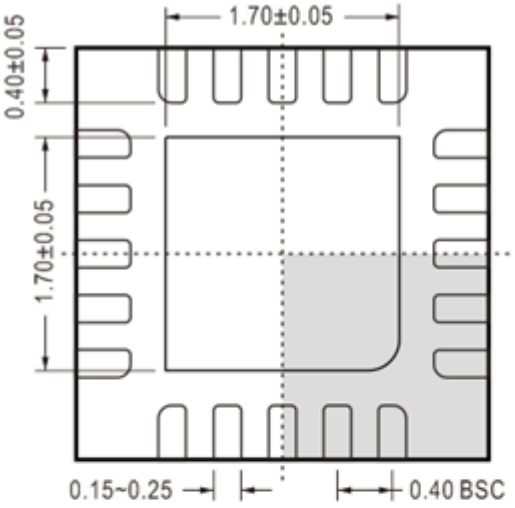
Charge Current vs Temperature



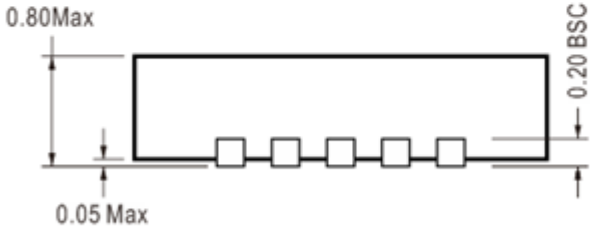
Package Information – WQFN3x3-20L

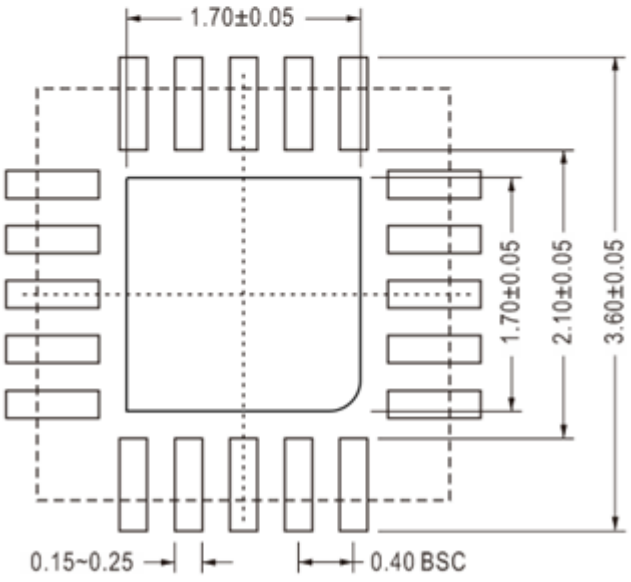
Unit: mm.





Bottom View - Exposed Pad





Recommended Solder Pad Pitch and Dimensions